ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

IPC-6012B
with Amendment 1

Qualification and Performance Specification for Rigid Printed Boards

IPC-6012B
with Amendment 1
January 2007

A standard developed by IPC

Supersedes IPC-6012B
August 2004

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IPC-6012B with Amendment 1

Qualification and Performance Specification for Rigid Printed Boards

Developed by the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) of IPC

Supersedes:

IPC-6012B - August 2004
IPC-6012A with
Amendment 1 - July 2000
IPC-6012A - October 1999
IPC-6012 - July 1996
IPC-RB-276 - March 1992

Users of this publication are encouraged to participate in the development of future revisions.

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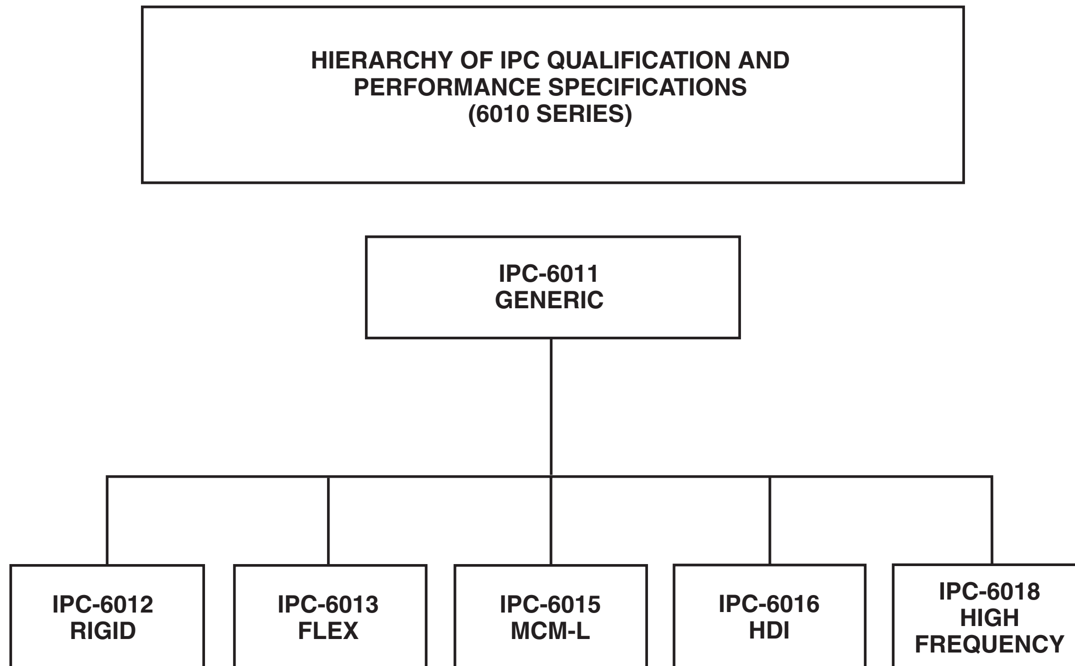

FOREWORD

This specification is intended to provide information on the detailed performance criteria of rigid printed boards. It supersedes IPC-6012B and was developed as a revision to those documents. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

Included in the set is the generic information, which is contained in the first document of the set. The generic specification is supplemented by one or multiple performance documents, each of which provide a specific focus on one aspect of the topic or the technology selected.

Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of ''Suggestions for Improvement'' forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Table of Contents

1 SCOPE ... 1
1.1 Statement of Scope ... 1
1.2 Purpose ... 1
1.3 Performance Classification and Type ... 1
1.3.1 Classification ... 1
1.3.2 Board Type ... 1
1.3.3 Selection for Procurement ... 1
1.3.4 Material, Plating Process and Final Finish ... 1
1.4 Definition of Terms ... 2
1.5 Interpretation ... 2
1.6 Revision Level Changes ... 2
2 APPLICABLE DOCUMENTS ... 2
2.1 IPC ... 3
2.2 Joint Industry Standards ... 4
2.3 Federal ... 4
2.4 Other Publications ... 4
2.4.1 American Society for Testing and Materials ... 4
2.4.2 Underwriters Lab ... 4
2.4.3 National Electrical Manufacturers Association ... 4
2.4.4 American Society for Quality ... 4
2.4.5 AMS ... 4
2.4.6 American Society of Mechanical Engineers ... 4
3 REQUIREMENTS ... 4
3.1 General ... 4
3.2 Materials Used in this Specification ... 4
3.2.1 Laminates and Bonding Material for Multilayer Boards ... 4
3.2.2 External Bonding Materials ... 4
3.2.3 Other Dielectric Materials ... 4
3.2.4 Metal Foils ... 4
3.2.5 Metal Planes/Cores ... 4
3.2.6 Metallic Platings and Coatings ... 5
3.2.7 Organic Solderability Preservative (OSP) ... 7
3.2.8 Polymer Coating (Solder Resist) ... 7
3.2.9 Fusing Fluids and Fluxes ... 7
3.2.10 Marking Inks ... 7
3.2.11 Hole Fill Insulation Material ... 7
3.2.12 Heatsink Planes, External ... 7
3.2.13 Via Protection ... 7
3.2.14 Embedded Passive Materials ... 7
3.3 Visual Examination ... 7
3.3.1 Edges ... 8
3.3.2 Laminate Imperfections ... 8
3.3.3 Plating and Coating Voids in the Hole ... 8
3.3.4 Lifted Lands ... 8
3.3.5 Marking ... 8
3.3.6 Solderability ... 9
3.3.7 Plating Adhesion ... 9
3.3.8 Edge Board Contact, Junction of Gold Plate to Solder Finish ... 9
3.3.9 Workmanship ... 9
3.4 Board Dimensional Requirements ... 9
3.4.1 Hole Size, Hole Pattern Accuracy and Pattern Feature Accuracy ... 10
3.4.2 Annular Ring and Breakout (External) ... 10
3.4.3 Bow and Twist ... 11
3.5 Conductor Definition ... 11
3.5.1 Conductor Width and Thickness ... 11
3.5.2 Conductor Spacing ... 11
3.5.3 Conductor Imperfections ... 11
3.5.4 Conductive Surfaces ... 12
3.6 Structural Integrity ... 13
3.6.1 Thermal Stress Testing ... 14
3.6.2 Requirements for Microsectioned Coupons or Production Boards ... 14
3.7 Solder Resist (Solder Mask) Requirements ... 20
3.7.1 Solder Resist Coverage ... 20
3.7.2 Solder Resist Cure and Adhesion ... 21
3.7.3 Solder Resist Thickness ... 21
3.8 Electrical Requirements ... 21
3.8.1 Dielectric Withstanding Voltage ... 21
3.8.2 Electrical Continuity and Insulation Resistance ... 21
3.8.3 Circuit/Plated-Through Shorts to Metal Substrate ... 21
3.8.4 Moisture and Insulation Resistance (MIR) ... 22
3.9 Cleanliness ... 22
3.9.1 Cleanliness Prior to Solder Resist Application ... 22
3.9.2 Cleanliness After Solder Resist, Solder, or Alternative Surface Coating Application ... 22
3.9.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination ... 22
3.10 Special Requirements ... 22
3.10.1 Outgassing ... 22
3.10.2 Organic Contamination ... 22
3.10.3 Fungus Resistance ... 22

3.10.4 Vibration 22
3.10.5 Mechanical Shock 23
3.10.6 Impedance Testing 23
3.10.7 Coefficient of Thermal Expansion (CTE) 23
3.10.8 Thermal Shock 23
3.10.9 Surface Insulation Resistance (As Received) 23
3.10.10 Metal Core (Horizontal Microsection) 23
3.10.11 Rework Simulation 23
3.10.12 Bond Strength, Unsupported Component Hole Land 23
3.11 Repair 23
3.11.1 Circuit Repairs 23
3.12 Rework 23

4 QUALITY ASSURANCE PROVISIONS 23
4.1 General 23
4.1.1 Qualification 24
4.1.2 Sample Test Coupons 24
4.2 Acceptance Tests 24
4.2.1 C=0 Zero Acceptance Number Sampling Plan 24
4.2.2 Referee Tests 24
4.3 Quality Conformance Testing 24
4.3.1 Coupon Selection 24

5 NOTES 29
5.1 Ordering Data 29
5.2 Superseded Specifications 29

IPC-6012B Performance Specification Sheet for Space and Military Avionics 30

APPENDIX A 35

Figures

Figure 3-1 Annular Ring Measurement (External) 11
Figure 3-2 Breakout of 90° and 180° 11
Figure 3-3 Conductor Width Reduction 11
Figure 3-4 Separations at External Foil 12
Figure 3-5 Crack Definition 13
Figure 3-6 Rectangular Surface Mount Lands 13
Figure 3-7 Round Surface Mount Lands 13
Figure 3-8 Typical Microsection Evaluation Specimen 16
Figure 3-9 Negative Etchback 16
Figure 3-10 Annular Ring Measurement (Internal) 17
Figure 3-11 Microsection Rotations for Breakout Detection 17
Figure 3-12 Comparison of Microsection Rotations 17
Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes) 18
Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable) 18
Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable) 18
Figure 3-16 Metal Core to Plated-Through Hole Spacing 19
Figure 3-17 Measurement of Minimum Dielectric Spacing 20

Tables

Table 1-1 Technology Adder Examples 1
Table 1-2 Default Requirements 2
Table 3-1 Internal or External Metal Planes 5
Table 3-2 Final Finish, Surface Plating and Coating Thickness Requirements 5
Table 3-3 Plating and Coating Voids Visual Examination 9
Table 3-4 Edge Board Contact Gap 9
Table 3-5 Minimum Annular Ring 10
Table 3-6 Plated Hole Integrity After Stress 15
Table 3-7 Internal Layer Foil Thickness after Processing 19
Table 3-8 External Conductor Thickness after Plating 19
Table 3-9 Solder Resist Adhesion 21
Table 3-10 Dielectric Withstanding Voltages 21
Table 3-11 Insulation Resistance 22
Table 4-1 Qualification Test Coupons 25
Table 4-2 C=0 Sampling Plan (Sample Size for Specific Index Value*) 25
Table 4-3 Acceptance Testing and Frequency 26
Table 4-4 Quality Conformance Testing 29

Qualification and Performance Specification for Rigid Printed Boards

1 SCOPE

1.1 Statement of Scope This specification covers qualification and performance of rigid printed boards. The printed board may be single-sided, double-sided, with or without plated-through holes. The printed board may be multilayer with plated-through holes and with or without buried/blind vias. The printed board may be multilayer containing build up HDI layers conforming to IPC-6016. The printed board may contain active embedded passive circuitry with distributive capacitive planes, capacitive or resistive components. The printed board may contain a metal core or external metal heat frame, which may be active or nonactive. Revision level changes are described in 1.6.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of rigid printed boards.

1.3 Performance Classification and Type

1.3.1 Classification This specification recognizes that rigid printed boards will be subject to variations in performance requirements based on end-use. The printed boards are classified by one of three general Performance Classes. Performance classes are defined in IPC-6011. Requirements deviating from these heritage classifications may be established through the use of a Performance Specification Sheet. Requirement exceptions commonly used for Space and Military avionics are shown as the Performance Specification Sheet Class 3A for Space and Military Avionics, listed in the back of this document.

1.3.2 Board Type Printed boards without plated-through holes (Type 1) and with plated-through holes (Types 2-6) are classified as follows:

Type 1—Single-Sided Board
Type 2—Double-Sided Board
Type 3—Multilayer board without blind or buried vias
Type 4—Multilayer board with blind and/or buried vias
Type 5—Multilayer metal core board without blind or buried vias
Type 6—Multilayer metal core board with blind and/or buried vias

1.3.3 Selection for Procurement For procurement purposes, performance class **shall** be specified in the procurement documentation. The documentation **shall** provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is shown in IPC-D-325.

1.3.3.1 Selection (Default) The procurement documentation should specify the requirements that can be selected within this specification; however, in the event selections are not made in the documentation, Table 1-2 **shall** apply.

1.3.3.2 Section System (Optional) The following product selection identifier system is provided for clarification of the build type.

Quality Specification, the generic quality specification.

Specification, the base performance specification.

Type, the product type per 1.3.2.

Plating Process, the plating process per 1.3.4.2.

Final Finish, the final finish code per 1.3.4.3.

Selective Finish, the selective finish code adder per 1.3.4.3, enter "-" when no selective finish is required.

Product Classification, the product classification per 1.3.1 or performance specification sheet.

Technology Adder, the technology adder as specified in Table 1-1. Add multiple codes as required.

Table 1-1 Technology Adder Examples

Technology Code	Technology
HDI	HDI build-up features per IPC-6016
VP	Via Protection
WBP	Wire Bondable Pads
AMC	Active Metal Core
NAMC	Nonactive Metal Core
HF	External Heat Frame
EP	Embedded Passives
VIP-C	Via-in-Pad, Conductive Fill
VIP-N	Via-in-Pad, Nonconductive Fill

Example: IPC 6011/6012/3/1/S/-/3/HDI/EP

1.3.4 Material, Plating Process and Final Finish

1.3.4.1 Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.

Table 1-2 Default Requirements

Category	Default Selection
Performance Class	Class 2
Material	Epoxy-Glass Laminate
Final Finish	Finish X (Electrodeposited tin lead, fused or solder coated)
Minimum Starting Foil	1/2 oz. For all internal and external layers except Type 1 which **shall** start with 1 oz.
Copper Foil Type	Electrodeposited
Hole Diameter Tolerance Plated, components Plated, via only Unplated	 (±) 100 µm [3,937 µin] (+) 80 µm [3,150 µin], (-) no requirement, (may be totally or partially plugged) (±) 80 µm [3,150 µin]
Conductor Width tolerance.	Class 2 requirements per para. 3.5.1
Conductor Spacing tolerance.	Class 2 requirements per para. 3.5.2
Dielectric Separation	90 µm [3,543 µin] minimum
Lateral Conductor Spacing	100 µm [3,937 µin] minimum
Marking Ink	Contrasting color, nonconductive
Solder Resist	Not applied, if not specified
Solder Resist, specified	Class T of IPC-SM-840 if class not specified
Solderability Test	Category 2 of J-STD-003
Test Voltage, Insulation Resistance	40 Volts
Qualification not specified	See IPC-6011

1.3.4.2 Plating Process The copper plating process, which is used to provide conductivity in the holes, is identified by a single number as follows:

1. Acid copper electroplating only
2. Pyrophosphate copper electroplating only
3. Acid and/or pyrophosphate copper electroplating
4. Additive/electroless copper
5. Electrodeposited Nickel underplate with acid and/or pyrophosphate copper electroplating

1.3.4.3 Final Finish The final finish can be but is not limited to one of the finishes specified below or a combination of several platings and is dependent on assembly processes and end-use. Thickness, where required, **shall** be specified in the procurement documentation unless listed in Table 3-2. Coating thickness may be exempted in Table 3-2 (i.e., tin-lead plate or solder coating). Designators for final finish are as follows:

S Solder Coating (Table 3-2)
T Electrodeposited Tin-Lead, (fused) (Table 3-2)
X Either Type S or T (Table 3-2)
TLU Electrodeposited Tin-Lead (unfused) (Table 3-2)
G Gold Electroplate for Edge Board Connectors (Table 3-2)
GS Gold Electroplate for Areas to be Soldered (Table 3-2)
GWB-1 Gold Electroplate for areas to be wire bonded (ultrasonic)
GWB-2 Gold Electroplate for areas to be wire bonded (thermosonic)
N Nickel for Edge Board Connectors (Table 3-2)
NB Nickel as a Barrier to Copper-Tin Diffusion (Table 3-2)
OSP Organic Solderability Protector (tarnish and Solderability protection during storage and assembly processes) (Table 3-2)
ENIG Electroless Nickel Immersion Gold (Table 3-2)
NBEG Nickel Barrier/Electroless Gold
IS Immersion Silver
IT Immersion Tin
C Bare Copper (Table 3-2)
SMOBC Solder Mask over Bare Copper
SMOBC - LPI Liquid Photoimageable Solder Mask over Bare Copper
SMOBC - DF Dry Film Solder Mask over Bare Copper
SMOBC - TM Thermal Mask Solder Mask over Bare Copper
Y Other

1.4 Definition of Terms The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined wherein.

Wire Bond Pad (WPB) Pads on a printed circuit board that are designed for wire-connections by thermo compression, ultrasonic, or related techniques. These pads are used for chip-on-board (COB) applications.

1.5 Interpretation ''Shall,'' the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a ''shall'' requirement may be considered if sufficient data is supplied to justify the exception.

The words ''should'' and ''may'' are used whenever it is necessary to express nonmandatory provisions.

''Will'' is used to express a declaration of purpose. To assist the reader, the word ''shall'' is presented in bold characters.

1.6 Revision Level Changes Changes made to this revision of the IPC-6012 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the Figure or Table header.

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent

specified herein. If a conflict of requirements exists between IPC-6012 and the listed applicable documents, IPC-6012 **shall** take precedence.

2.1 IPC[1]

IPC-A-47 Composite Test Pattern Ten Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-DD-135 Qualification for Deposited Organic Interlayer Dielectric Materials for Multichip Modules

IPC-CF-148 Resin Coated Metal for Printed Boards

IPC-CF-152 Composite Material Specifications for Printed Wiring Boards

IPC-D-325 Documentation Requirements for Printed Boards, Assemblies, and Support Drawings

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual[2]

2.1.1E	05/04	Microsectioning
2.1.1.2A	05/04	Microsectioning, Semi or Automatic Technique Microsection Equipment (Alternate)
2.3.15D	05/04	Purity, Copper Foil or Plating
2.3.25C	02/01	Detection and Measurement of Ionizable Surface Contaminants
2.3.38C	05/04	Surface Organic Contaminant Detection Test
2.3.39C	05/04	Surface Organic Contaminant Identification Test (Infrared Analytical Method)
2.4.1E	05/04	Adhesion, Tape Testing
2.4.15A	03/76	Surface Finish, Metal Foil
2.4.18.1A	05/04	Tensile Strength and Elongation, In-House Plating
2.4.21E	05/04	Land Bond Strength, Unsupported Component Hole
2.4.22C	06/99	Bow and Twist
2.4.28.1D	05/04	Adhesion, Solder Resist (Mask), Tape Test Method
2.4.36C	05/04	Rework Simulation, Plated-Through Holes for Leaded Components
2.4.41.2A	05/04	Coefficient of Thermal Expansion, Strain Gage Method
2.5.5.7A	03/04	Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR
2.5.7D	05/04	Dielectric Withstand Voltage, PWB
2.6.1F	05/04	Fungus Resistance, Printed Wiring Materials
2.6.3F	05/04	Moisture and Insulation Resistance, Rigid Boards
2.6.4B	05/04	Outgassing, Printed Boards
2.6.5D	05/04	Physical Shock, Multilayer Printed Wiring
2.6.7.2B	05/04	Thermal Shock, Continuity and Microsection, Printed Boards
2.6.8E	05/04	Thermal Stress, Plated-Through Holes
2.6.9B	05/04	Vibration, Rigid Printed Wiring

IPC-QL-653 Certification of Facilities that Inspect/Test Printed Wiring Boards, Components and Materials

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-2221 Generic Standard on Printed Board Design

IPC-2251 Design Guide for the Packaging of High Speed Electronic Circuits

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films

IPC-4552 Electroless Nickel/Immersion Gold Plating for Electronic Interconnections

IPC-4553 Specification for Immersion Silver Plating for Printed Circuit Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6015 Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-6018 Microwave End Product Board Inspection and Test

1. www.ipc.org
2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm)

IPC-7711/21A Repair and Rework Guide

IPC-9151 Printed Board Process, Capability, Quality and Relative Reliability (PCQR^2) Benchmark Test Standard and Database

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

2.2 Joint Industry Standards[3]

J-STD-003 Solderability Tests for Printed Boards

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.3 Federal[4]

QQ-S-635 Steel

2.4 Other Publications

2.4.1 American Society for Testing and Materials[5]

ASTM B-152 Standard Specification for Copper Sheet, Strip, Plate and Rolled Bar

ASTM B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses

ASTM B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.4.2 Underwriters Lab[6]

UL 94 Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

2.4.3 National Electrical Manufacturers Association[7]

NEMA LI-1 Industrial Laminate Thermosetting Product

2.4.4 American Society for Quality[8]

H0862 Zero Acceptance Number Sampling Plans

2.4.5 AMS[9]

SAE-AMS-QQ-A-250 Aluminum Alloy, Plate and Sheet

SAE-AMS-QQ-N-290 Nickel Plating (Electrodeposited)

2.4.6 American Society of Mechanical Engineers[10]

ASME B46.1 Surface Texture (Surface Roughness, Waviness and Lay)

3 REQUIREMENTS

3.1 General Printed boards furnished under this specification **shall** meet or exceed the requirements of IPC-6011 and the specific performance class as required by the procurement documentation. Descriptions and purposes of test coupons are documented in IPC-2221.

3.2 Materials Used in this Specification

3.2.1 Laminates and Bonding Material for Multilayer Boards Metal clad laminates, unclad laminates and bonding material (prepreg) should be selected from IPC-4101, IPC-4202, IPC-4203, or NEMA LI-1. Polytetrafluoroethylene (PTFE) material types should be selected from IPC-4103. Embedded Passives materials should be as specified in the procurement documentation including dielectric, conductive, resistive and insulating characteristics as applicable. The specification sheet number, metal cladding type and metal clad thickness (weight) **shall** be as specified in the procurement documentation. When specific requirements such as the flammability requirements shown in UL 94 for laminate and bonding materials are required, it is necessary to specify those requirements in material procurement documents.

3.2.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners to the printed board **shall** be selected from IPC-4101, IPC-4203 or as specified in the procurement documentation.

3.2.3 Other Dielectric Materials Photoimageable dielectrics should be selected from IPC-DD-135 and specified in the procurement documentation. Other dielectric materials may be specified in the procurement documentation.

3.2.4 Metal Foils Copper foil **shall** be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment and foil profile should be specified on the master drawing if critical to the function of the printed board. Resin coated copper foil **shall** be in accordance with IPC-CF-148.

3.2.4.1 Resistive Metal Foil Resistive metal foil **shall** be specified in the procurement documentation.

3.2.5 Metal Planes/Cores Metal planes and/or metal core substrates **shall** be specified on the master drawing as shown in Table 3-1.

3. www.ipc.org
4. www.sae.org
5. www.astm.org
6. www.ul.com
7. www.nema.org
8. www.asq.org
9. www.sae.org
10. www.asme.org

Table 3-1 Internal or External Metal Planes

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As Specified
Steel	QQ-S-635	As Specified
Copper	ASTM-B-152 or IPC-4562	As Specified
Copper-Invar-Copper	IPC-CF-152	As Specified
Copper-Moly-Copper	IPC-CF-152	As Specified
Other	As Specified	As Specified

3.2.6 Metallic Platings and Coatings Thickness of the plating/coating **shall** be in accordance with Table 3-2. The copper plating thickness on the surface, in plated-through holes, via holes and in blind and buried vias **shall** be as specified in Table 3-2. Thickness of platings for a specific use is shown in Table 3-2. Final finishes selected from those listed in 1.3.4.3 or combinations required **shall** specify plating thickness except for fused tin-lead plating or solder coating which requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges; conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.4.7.

Note: The Category of solderability testing **shall** be specified by the user per J-STD-003; however, in the event it is not specified the supplier **shall** test to Category 2 (steam aging is not required).

3.2.6.1 Electroless Depositions and Conductive Coatings Electroless depositions and conductive coatings **shall** be sufficient for subsequent plating processes and may be either electroless metal, vacuum deposited metal, or metallic or nonmetallic conductive coatings. Electroless nickel/immersion gold plating (ENIG) **shall** be in accordance with IPC-4552. Measurement location and extent **shall** be AABUS.

Caution: Immersion gold thicknesses above 0.125 µm [4.925 µin] can indicate an increased risk of having compromised the integrity of the nickel undercoat due to excessive corrosion. Due to the influence of the design pattern and chemistry process variability, acceptance of the solderability coupon may not represent the part. Correlation of thickness measurements across the pattern is strongly encouraged to demonstrate uniformity of the coating thickness.

3.2.6.2 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

3.2.6.3 Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-2 applies.

3.2.6.4 Solder Coating The solder used for solder coating **shall** be Sn60A, Sn60C, Pb40A, Pb36A, Pb36B, Pb36C, Sn63A, Sn63C or Pb37A per J-STD-006.

3.2.6.5 Nickel Nickel plating **shall** be in accordance with SAE-AMS-QQ-N-290 Class 2, except the thickness **shall** be in accordance with Table 3-2.

3.2.6.6 Electrodeposited Gold Plating Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Purity, hardness and thickness **shall** be specified in the procurement documentation. For Class 3 boards, gold plating **shall** be Type 1 or 3, Class 1. Gold plating thickness on areas to be wire bonded **shall** be as specified in Table 3-2.

Table 3-2 Final Finish, Surface Plating and Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage & Solderable[4]	Coverage & Solderable[4]	Coverage & Solderable[4]
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable[4]	Coverage & Solderable[4]	Coverage & Solderable[4]
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold for edge-board connectors and areas not to be soldered - minimum	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold on areas to be soldered - maximum	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) - minimum	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]

Code	Finish	Class 1	Class 2	Class 3
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]
N	Nickel - Electroplate for Edge Board Connectors - minimum	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier[1] - minimum	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	Organic Solderability Preservative	Solderable[4]	Solderable[4]	Solderable[4]
ENIG	Electroless Nickel - minimum	3 µm [118 µin]	3 µm [118 µin]	3 µm [118 µin]
	Immersion Gold (Solderable Surface)	Solderable[6]	Solderable[6]	Solderable[6]
	Immersion Gold (Other) - minimum	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
IS	Immersion Silver	Solderable[4,7]	Solderable[4,7]	Solderable[4,7]
IT	Immersion Tin	Solderable[4]	Solderable[4]	Solderable[4]
C	Bare Copper	As indicated in Table 3-7 and/or Table 3-8		
Through-Holes				
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin areas	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]
Blind Vias				
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]
Microvias[3] (Blind and Buried)				
	Copper[2] - minimum average	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Minimum thin area	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	6 µm [236 µin]
Buried Via Cores				
	Copper[2] - minimum average	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	Minimum thin area	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	7 µm [276 µin]
Buried Vias (>2 layers)				
	Copper[2] - minimum average	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Minimum thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Minimum Wrap[5]	AABUS	5 µm [197 µin]	12 µm [472 µin]

[1]Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
[2]Copper plating (1.3.4.2) thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 section on copper plating thickness for hole walls.
[3]Blind microvias are vias that <0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink-formation followed by a plating operation. All performance characteristics for plated holes, as defined in this document, **shall** be met. The values given for blind and buried microvias in Table 3-2 are not applicable for stacked microvias. As of the publication of this specification, there is little known about this structure and the reliability results are not consistent with buried and blind microvias. Stacked microvias may also require different inspection criteria.
[4]See also 3.3.6.
[5]Wrap copper plating for filled plated holes **shall** be in accordance with 3.6.2.11.1.
[6]See also 3.2.6.1.
[7]See also 3.2.6.7.

3.2.6.7 Immersion Silver Plating Immersion silver plating **shall** be in accordance with IPC-4553. Unlike other surface finishes, immersion silver plating is available in two very distinctive but acceptable versions - a thin silver deposit and a thicker silver deposit. It is imperative that the supplier of the printed circuit boards inform the user of the immersion silver plating as to which type of silver they are supplying. Surface thickness measurements, when required for immersion silver, **shall** be in accordance with IPC-4553.

NOTE: Pad size for thickness measurements are defined in IPC-4553 and apply for both thin and/or thick silver deposits. Immersion silver finishes are not recommended for ''contact surfaces'' of Class 3 products.

3.2.6.8 Other Metals and Coatings Other depositions such as bare copper, palladium, rhodium, tin, solder alloys, etc., may be used provided they are specified in the procurement documentation.

3.2.6.9 Electrodeposited Copper When specified, electrodeposited copper platings **shall** meet the following criteria. Frequency of testing **shall** be determined by the manufacturer to ensure process control.

a) When tested as specified in IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50%.

b) When tested as specified in IPC-TM-650, Method 2.4.18.1, with the exception of removing the bake step in Section 5 within the test method, using 50 µm - 100 µm [1,969 µin - 3,937 µin] thick samples, the tensile strength **shall** be no less than 36,000 PSI [248 MPa] and the elongation **shall** be no less than 12%.

3.2.7 Organic Solderability Preservative (OSP) OSPs are anti-tarnish and solderability protectors applied to copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. Specific solderability shelf-life and soldering cycle requirements, if applicable, **shall** be specified in the procurement documentation.

3.2.8 Polymer Coating (Solder Resist) When permanent solder resist coating is specified, it **shall** be a polymer coating conforming to IPC-SM-840. (See 3.7 for solder resist coverage.)

3.2.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning and fusing the tin-lead plating and bare copper to allow for a smooth adherent coating. The fusing fluid **shall** act as a heat transfer and distribution medium to prevent damage to the bare laminate of the board.

Note: Fusing fluid compatibility should be confirmed with end users' cleanliness requirements due to the diverse interactions experienced at assembly soldering.

3.2.10 Marking Inks Marking inks **shall** be permanent, nonnutrient polymer inks, and **shall** be specified in the procurement documentation. Marking inks **shall** be applied to the board, or to a label applied to the board. Marking inks and labels must be capable of withstanding fluxes, cleaning solvents, soldering, cleaning and coating processes encountered in later manufacturing processes. If a conductive marking ink is used, the marking **shall** be treated as a conductive element on the board.

3.2.11 Hole Fill Insulation Material Electrical insulation material used for hole-fill for metal core printed boards **shall** be as specified in the procurement documentation.

3.2.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes **shall** be as specified in Table 3-1 and/or the procurement documentation. Bonding material **shall** be as specified in 3.2.2 and/or the procurement documentation.

3.2.13 Via Protection Materials for accomplishing via protection method **shall** be as specified in the procurement documentation.

3.2.14 Embedded Passive Materials Embedded passive materials are defined as materials and processes which add capacitive, resistive and/or inductive functionality within the printed circuit board, and which may be used with conventional core materials for the manufacture of printed circuit boards. These include laminate materials, resistive metal foils, plated resistors, conductive pastes, protectant materials, etc. Embedded passive materials **shall** be as specified in the procurement documentation. At the time of publication to the B Revision to the IPC-6012, standards efforts involving design requirements, material specification and finished printed board acceptance criteria involving embedded passive technology were underway and intended for future incorporation in IPC-2220 and IPC-6010 series documentation. IPC maintains a listing for the activities under the D-37 Embedded Passives subcommittee at www.ipc.org/committeepage.asp.

3.3 Visual Examination Finished printed boards **shall** be examined in accordance with the following procedure. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.9.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx.1.75X). If confirmation of a suspected defect cannot be made at 3 diopters, it should be verified at progressively higher magnifications (up to 40X)

to confirm that it is a defect. Dimensional requirements such as spacing or conductor width measurements may require other magnifications and devices with reticles or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

3.3.1 Edges Nicks, crazing or haloing along the edge of the board, edge of cutouts and edges of nonplated-through holes are acceptable provided the penetration does not exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less. Edges **shall** be clean cut and without metallic burrs. Nonmetallic burrs are acceptable as long as they are not loose and/or do not affect fit and function. Panels, which are scored or routed with a breakaway tab, **shall** meet the depanelization requirements of the assembled board.

3.3.2 Laminate Imperfections Laminate imperfections include those characteristics that are both internal and external within the printed board but are visible from the surface.

3.3.2.1 Measling Measling is acceptable for Class 1, 2 and 3 end product, with the exception of high-voltage applications as defined by the customer. Refer to IPC-A-600 for more information.

Note: The reader should be aware that, at the time of publication of this amendment to this specification, the IPC-A-610 and IPC-J-STD-001 assembly standards take exception to the bare board measling criteria for Class 3 in this specification.

3.3.2.2 Crazing Crazing is acceptable for all classes of end product provided the imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates future assembly processes. For Class 2 and 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors. Refer to IPC-A-600 for more information.

3.3.2.3 Delamination/Blister Delamination and blistering is acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates future assembly processes. For Class 2 and 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns. Refer to IPC-A-600 for more information.

3.3.2.4 Foreign Inclusions Translucent particles trapped within the board **shall** be acceptable. Other particles trapped within the board **shall** be acceptable, provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.

3.3.2.5 Weave Exposure Weave exposure or exposed/disrupted fibers are acceptable for all Classes provided the imperfection does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum. Refer to IPC-A-600 for more information.

3.3.2.6 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable provided they do not bridge conductors or expose/disrupt fibers greater than allowed in the paragraphs above and do not reduce the dielectric spacing below the minimum specified.

3.3.2.7 Surface Voids Surface voids are acceptable provided they do not exceed 0.8 mm [0.031 in] in the longest dimension; bridge conductors; or exceed 5% of the total board area per side.

3.3.2.8 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall not** exceed 10% of the total conductor surface area of the affected layer.

3.3.2.9 Pink Ring No evidence exists that pink ring affects functionality. The presence of pink ring may be considered an indicator of process or design variation but is not a cause for rejection. The focus of concern should be the quality of the lamination bond.

3.3.3 Plating and Coating Voids in the Hole Plating and coating voids **shall not** exceed that allowed by Table 3-3.

3.3.4 Lifted Lands When visually examined in accordance with 3.3, there **shall** be no lifted lands on the delivered (nonstressed) printed circuit board.

3.3.5 Marking Each individual board, each qualification board, and quality conformance test circuitry (as opposed to each individual test coupon) **shall** be marked in order to insure traceability between the boards/quality conformance test circuitry and the manufacturing history and to identify the supplier (logo, etc.). The marking **shall** be produced by the same process as used in producing the conductive pattern, or by use of a permanent fungistatic ink or paint (see 3.2.10), LASER marker or by vibrating pencil marking on a metallic area provided for marking purposes or a permanently attached label. Conductive markings, either etched copper or conductive ink (see 3.2.10) **shall** be considered as electrical elements of the circuit and **shall not** reduce the electrical spacing requirements. All markings **shall** be compatible with materials and parts, legible for all tests,

Table 3-3 Plating and Coating Voids Visual Examination

Material	Class 1	Class 2	Class 3
Copper[1]	Three voids allowed per hole in not more than 10% of the holes.	One void allowed per hole in not more than 5% of the holes.	None
Finish Coating[2]	Five voids allowed per hole in not more than 15% of the holes.	Three voids allowed per hole in not more than 5% of the holes.	One void allowed per hole in not more than 5% of the holes.

[1] For class 2 product, copper voids **shall not** exceed 5% of the hole length. For class 1 product, copper voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° of the circumference.
[2] For class 2 and 3 product, finished coating voids **shall not** exceed 5% of the hole length. For class 1, finished coating voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° for class 1, 2 or 3.

and in no case affect board performance. Marking **shall not** cover areas of lands that are to be soldered. Refer to IPC-A-600 for legibility requirements. In addition to this marking, the use of bar code marking is permissible. When used, date code **shall** be formatted per the suppliers discretion in order to establish traceability as to when the manufacturing operations were performed.

3.3.6 Solderability Only those printed boards that require soldering in a subsequent assembly operation require solderability testing. Boards that do not require soldering do not require solderability testing and this **shall** be specified on the master drawing, as in the case where press-fit components are used. Boards to be used only for surface mount do not require hole solderability testing. When required by the procurement documentation, accelerated aging for coating durability **shall** be in accordance with J-STD-003. The Category of durability **shall** be specified on the master drawing; however, if not specified, Category 2 **shall** be used. Test coupons or production boards to be tested **shall** be conditioned, if required, and evaluated for surface and hole solderability using J-STD-003.

When solderability testing is required, consideration should be given to board thickness and copper thickness. As both increase, the amount of time to properly wet the sides of the holes and the tops of the lands increases proportionately.

Note: Accelerated aging (steam aging) is intended for use on coatings of tin/lead, tin/lead solder or tin, but not other final finishes.

3.3.7 Plating Adhesion Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape applied to the surface and removed by manual force applied perpendicular to the circuit pattern.

There **shall** be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal (slivers) breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of plating adhesion failure.

3.3.8 Edge Board Contact, Junction of Gold Plate to Solder Finish Exposed copper/plating overlap between the solder finish and gold plate **shall** meet the requirements of Table 3-4. The exposed copper/plating or gold overlap may exhibit a discolored or gray-black area which is acceptable (see 3.5.4.4).

Table 3-4 Edge Board Contact Gap

	Max. Exposed Copper Gap	Max. Gold Overlap
Class 1	2.5 mm [0.0984 in]	2.5 mm [0.0984 in]
Class 2	1.25 mm [0.04921 in]	1.25 mm [0.04291 in]
Class 3	0.8 mm [0.031 in]	0.8 mm [0.031 in]

3.3.9 Workmanship Printed boards **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, tin/lead or solder smear transfer to the dielectric surface, flux residue and other contaminants that affect life, ability to assemble and serviceability. Visually dark appearances in nonplated holes, which are seen when a metallic or non-metallic semiconductive coating is used, are not foreign material and do not affect life or function. Printed boards **shall** be free of defects in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the printed board.

3.4 Board Dimensional Requirements Inspection of dimensional requirements **shall** be as defined herein unless otherwise agreed upon between user and supplier. The board **shall** meet the dimensional requirements specified in the procurement documentation. All dimensional characteristics such as, but not limited to, board periphery, thickness, cutouts, slots, notches, holes, scoring and edge board contacts to connector key area **shall** be as specified in the procurement documentation. However, in the event that dimensional tolerances are not specified in the procurement documentation, the applicable feature tolerances of the IPC-2220 design series **shall** apply. Board dimensional locations of basic or bilateral tolerance as defined in the procurement documentation **shall** be inspected in accordance with the applicable AQL classification as specified in Table 4-3.

Automated inspection technology is allowed.

Table 3-5 Minimum Annular Ring

Characteristic	Class 1	Class 2	Class 3
External Plated-through holes	Not greater than 180° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [1,969 µin] or the minimum line width, whichever is smaller.	The minimum annular ring **shall** be 50 µm [1,969 µin]. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
Internal Plated-through holes	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.[1]	90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.[1]	The minimum internal annular ring **shall** be 25 µm [984 µin].
External Unsupported holes	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	The minimum annular ring **shall** be 150 µm [5,906 µin]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

[1]Minimum lateral spacing **shall** be maintained.

Note: (see Figure 3-2 and 3-3 for visual examples of land breakout and conductor width reduction at land).

Supplier in-process certification of features of accuracy to reduce inspection is allowed provided the method is documented and demonstrates capability to meet the specified requirements. The supplier may provide a statement of certification of accuracy based on the suppliers sampling plan which includes a process data collection and recording system.

In the event that the supplier does not have a process certification system for dimensional accuracy the AQL levels of Table 4-3 **shall** apply for each production lot.

3.4.1 Hole Size, Hole Pattern Accuracy and Pattern Feature Accuracy The hole size tolerance, hole pattern accuracy and feature location accuracy **shall** be as specified in the procurement documentation.

Finished hole size tolerance **shall** be verified on a sample basis across all hole sizes applicable to the design. The number of measures per hole size **shall** be determined by the manufacturer to adequately sample the quantity of holes within the population.

Only specific dimensioned holes, to include both nonplated-through and plated-through, **shall** be inspected for hole pattern accuracy to meet board dimensional requirements of 3.4. Unless required by the master drawing, hole pattern accuracy for other nonspecifically dimensioned holes, such as plated-through holes and vias, need not be checked as they are database supplied locations and are controlled by annular ring requirements to surface or internal lands. If required by master drawing, hole pattern accuracy may be certified by a statement of qualification or by AQL sampling per 3.4.

Pattern feature accuracy **shall** be as specified in the procurement documentation. Pattern feature accuracy may be certified through a statement of qualification or by AQL sampling per 3.4. However, in the event that any of these characteristics are not specified in the procurement documentation, the applicable IPC-2220 design series **shall** apply. Automated inspection technology is allowed.

Nodules or rough plating in plated-through holes **shall not** reduce the hole diameter below the minimum limits defined in the procurement document.

3.4.2 Annular Ring and Breakout (External) The minimum external annular ring **shall** meet the requirements of Table 3-5. The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole, or unsupported hole, to the outer edge of the annular ring on the surface of the board as shown in Figure 3-1. For Class 1 and 2, external plated through holes identified as vias (not having a component) can have up to 90° breakout of the annular ring. The break out **shall not** occur at the conductor/land intersection and the hole **shall** meet the requirements of 3.6.2.1 and 3.6.2.2. The finished board with the related breakout **shall** meet the electrical requirements of 3.8.2 (see Figures 3-2 and 3-3). Unless prohibited by the customer, the employment of filleting or ''tear drops'' to create additional land area at the conductor junction **shall** be acceptable for Class 1 and 2 and in accordance with general requirements for lands with holes

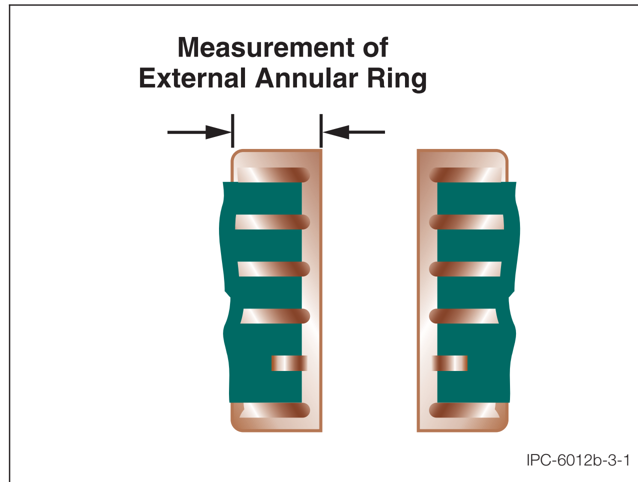

Figure 3-1 Annular Ring Measurement (External)

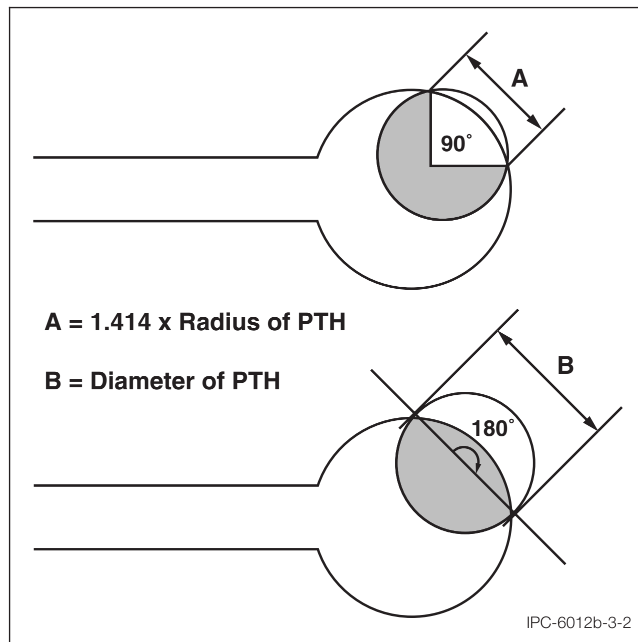

Figure 3-2 Breakout of 90° and 180°

detailed in IPC-2221. Employment of filleting or ''tear drops'' in Class 3 product **shall** be as agreed upon between user and supplier.

3.4.3 Bow and Twist Unless otherwise specified in the procurement documentation, when designed in accordance with 5.2.4 of IPC-2221, the printed board **shall** have a maximum bow and twist of 0.75% for boards that use surface mount components and 1.5% for all other boards. End products **shall** be assessed in the delivered form.

Bow, twist, or any combination thereof, **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22.

3.5 Conductor Definition All conductive areas on printed boards including conductors, lands and planes **shall** meet the visual and dimensional requirements of the following sections. The conductor pattern **shall** be as specified in the procurement documentation. Verification of dimensional attributes **shall** be performed in accordance with 3.3 and IPC-A-600. AOI inspection methods are allowed. Internal conductors are examined during internal layer processing prior to multilayer lamination.

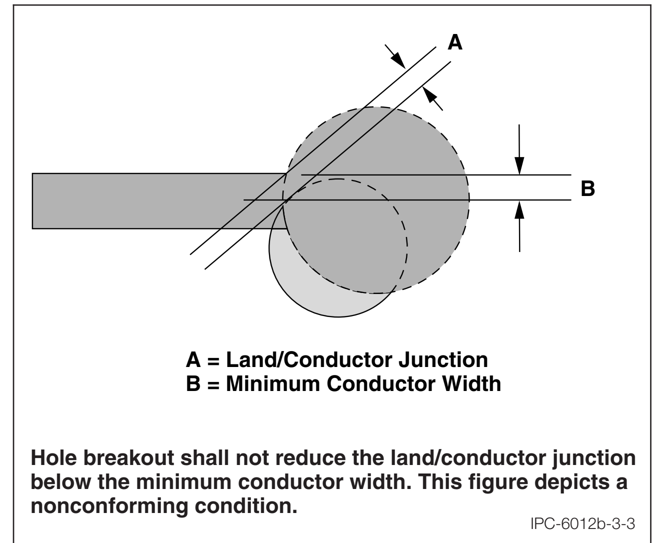

Figure 3-3 Conductor Width Reduction

3.5.1 Conductor Width and Thickness When not specified on the master drawing the minimum conductor width **shall** be 80% of the conductor pattern supplied in the procurement documentation. When not specified on the master drawing, the minimum conductor thickness **shall** be in accordance with 3.6.2.12 and 3.6.2.13.

3.5.2 Conductor Spacing The conductor spacing **shall** be within the tolerance specified on the master drawing. Minimum spacing between the conductor and the edge of the board **shall** be as specified on the master drawing.

If minimum spacing is not specified, the allowed reduction in the nominal conductor spacings shown in the engineering documentation due to processing **shall** be 20% for Class 3 and 30% for Class 1 and 2 (minimum product spacing requirements as previously stated apply).

3.5.3 Conductor Imperfections The conductive pattern **shall** contain no cracks, splits or tears. The physical geometry of a conductor is defined by its width x thickness x length. Any combination of defects specified in 3.5.3.1 and 3.5.3.2 **shall not** reduce the equivalent cross sectional area (width x thickness) of the conductor by more than 20% of the minimum value (minimum thickness x minimum width) for Class 2 and 3, and 30% of the minimum value for Class 1. The total combination of defect area lengths on a conductor **shall not** be greater than 10% of the conductor length or 25 mm [0.984 in] (for Class 1) or 13 mm [0.512 in] (for Class 2 or 3), whichever is less.

3.5.3.1 Conductor Width Reduction Allowable reduction of the minimum conductor width (specified or derived) due to misregistration or isolated defects (i.e., edge roughness, nicks, pinholes and scratches) which exposes base material **shall not** exceed 20% of the minimum conductor width for Class 2 and 3, and 30% of the minimum conductor width for Class 1.

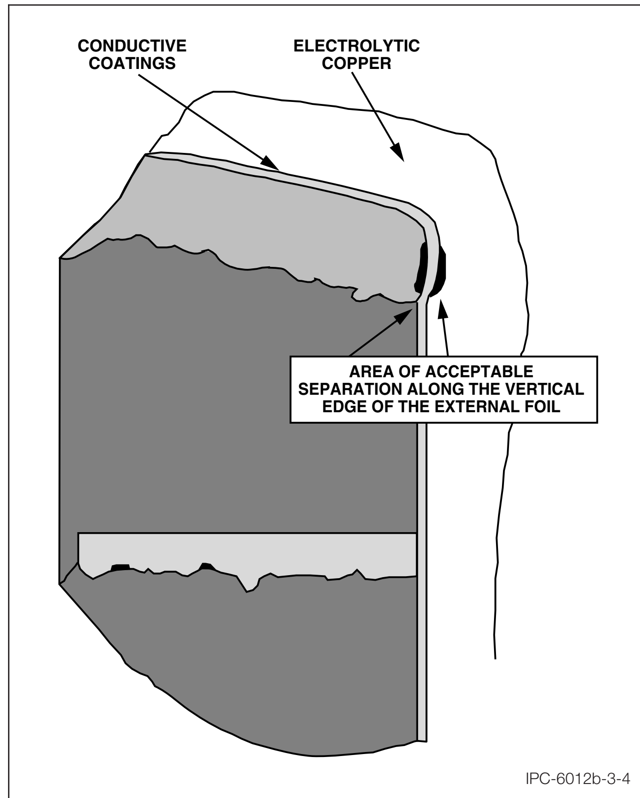

Figure 3-4 Separations at External Foil

3.5.3.2 Conductor Thickness Reduction Allowable reduction of the minimum conductor thickness due to isolated defects (i.e., edge roughness, nicks, pinholes, depressions and scratches) **shall not** exceed 20% of the minimum conductor thickness for Class 2 and 3, and 30% of the minimum conductor thickness for Class 1.

3.5.4 Conductive Surfaces

3.5.4.1 Nicks and Pinholes in Ground or Voltage Planes Nicks and pinholes are acceptable in ground or voltage planes for Class 2 and 3 if they do not exceed 1.0 mm [0.0394 in] in their longest dimension and there are no more than four per side per 625 cm^2 [96.88 in^2]. For Class 1, the longest dimension **shall** be 1.5 mm [0.0591 in] with no more than six per side, per 625 cm^2 [96.88 in^2].

3.5.4.2 Solderable Surface Mount Lands Defects along the edge of the land or internal to the land **shall not** exceed the requirements in 3.5.4.2.1 through 3.5.4.2.2.

3.5.4.2.1 Rectangular Surface Mount Lands Defects such as nicks, dents, and pin holes along the external edge of the land **shall not** exceed 20% of either the length or width of the land for Class 2 or Class 3 boards, or 30% for Class 1, and **shall not** encroach the pristine area, which is defined by the central 80% of the land width by 80% of the land length as shown in Figure 3-6. Defects internal to the land **shall not** exceed 10% of the length or width of the land for Class 2 or Class 3 boards, or 20% for Class 1, and **shall** remain outside of the pristine area of the surface mount land. One electrical test probe ''witness'' mark is allowed within the pristine area for Class 1, 2 and 3.

3.5.4.2.2 Round Surface Mount Lands (BGA Pads) Defects such as nick, dents and pin holes along the edge of the land **shall not** radially extend towards the center of the land by more than 10% of the diameter of the land for Class 1, 2 or 3 boards and **shall not** extend more than 20% around the circumference of the land for Class 2 or 3 boards or 30% for Class 1 as shown in Figure 3-7. There **shall** be no defects within the pristine area which is defined by the central 80% of the land diameter. One electrical test probe ''witness'' mark is allowed within the pristine area for Class 1, 2 and 3.

3.5.4.3 Wire Bond Pads (WBP) The wire bond pad **shall** have a final conductor finish as specified in 1.3.4.2 for ultrasonic (GWB-1) and thermosonic (GWB-2) wire bonding of gold electroplate or electroless nickel/immersion gold (ENIG), or as specified in the procurement documentation. The final finish coating thickness **shall** be per Table 3-2 for the applicable coating used. The pristine area **shall** consist of the central 80% of the pad width by 80% of the pad length of the wire bond pad as shown in Figure 3-6. The maximum surface roughness in the pristine area of the wire bond pad **shall** be measured in accordance with an applicable test method as agreed upon between user and supplier and **shall** be 0.8 µm [32 µin] RMS (Root-Mean-Square). If using IPC Method 2.4.15, it is recommended that the roughness-width cutoff identified in Method 2.4.15 be adjusted to approximately 80% of the maximum length of the wire bond pad in order to obtain the RMS value within the pristine area. There **shall** be no pits, nodules, scratches, electrical test probe ''witness'' marks, or other defects in the pristine area that violate the 0.8 µm [32 µin] RMS roughness requirement. For more information on surface roughness, refer to ASME B46.1.

3.5.4.4 Edge Board Connector Lands On gold or other noble metal plated edge board connector lands, except as noted below, the insertion or critical contact area **shall** be free of cuts or scratches that expose underlying nickel or copper, solder splashes or tin-lead plating, and nodules or metal bumps that protrude above the surface. Pits, dents or depressions are acceptable if they do not exceed 0.15 mm [0.00591 in] in their longest dimension and there are not more than three per land and do not appear on more than

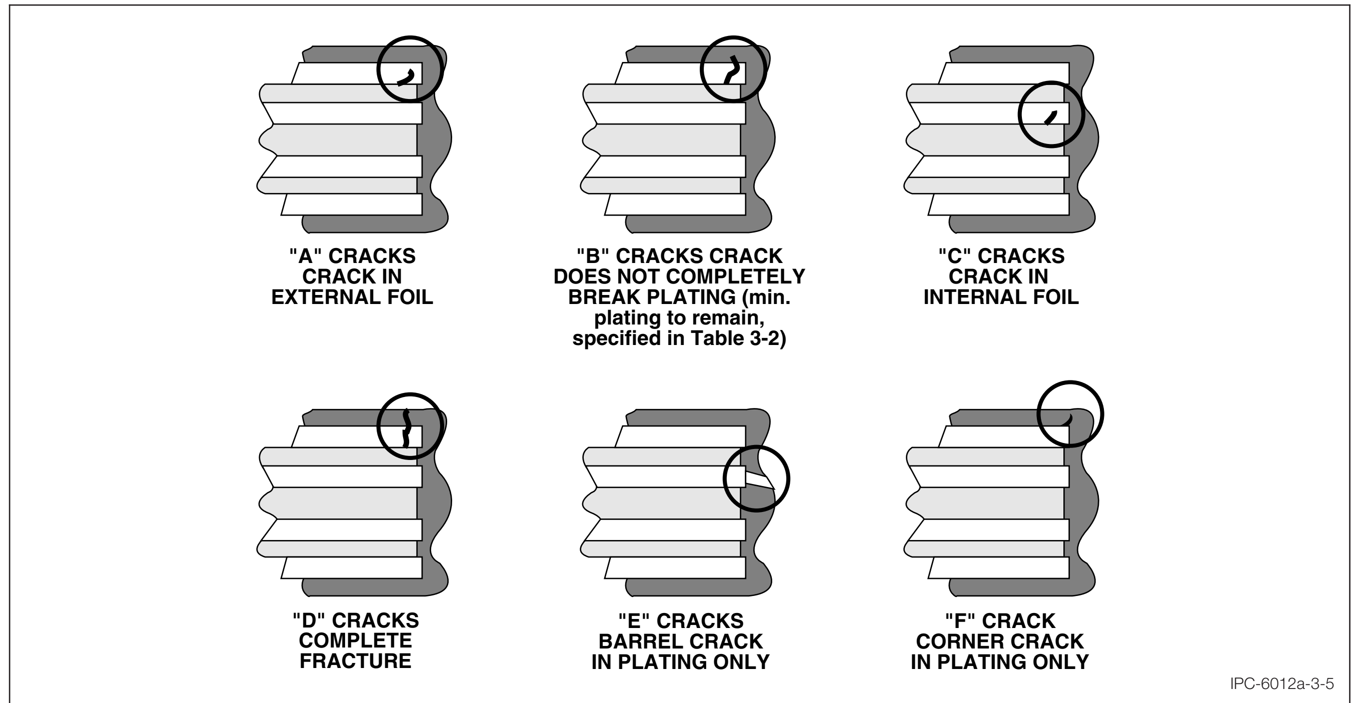

Figure 3-5 Crack Definition

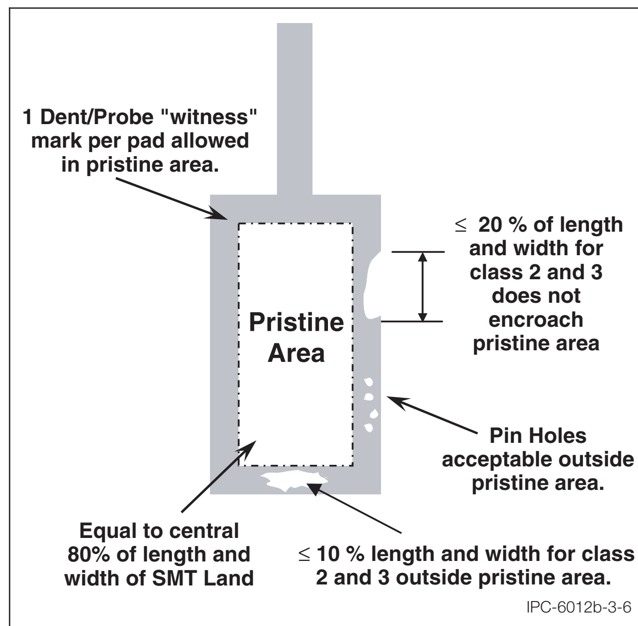

Figure 3-6 Rectangular Surface Mount Lands

30% of the lands. The imperfection limits do not apply to a band 0.15 mm [0.00591 in] wide around the perimeter of the land including the critical contact area.

3.5.4.5 Dewetting For tin, tin/lead reflowed, or solder coated surfaces, dewetting on conductors, areas of solder connection, and ground or voltage planes is allowed to the extent listed below:

a. Conductors and planes—permitted for all classes.

b. Individual areas of solder connection – Class 1–15%; Class 2–5%; Class 3–5%.

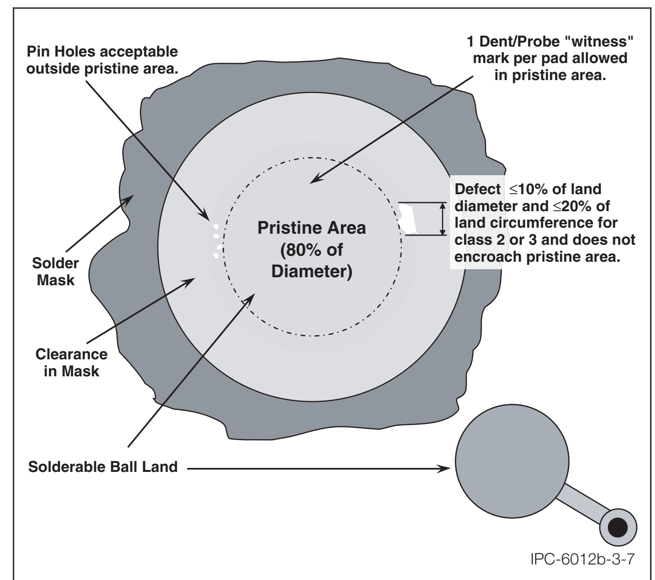

Figure 3-7 Round Surface Mount Lands

3.5.4.6 Nonwetting For tin, tin/lead reflowed or solder coated surfaces; nonwetting is not permitted on any conductive surface where a solder connection will be required.

3.5.4.7 Final Finish Coverage (Areas not to be soldered) Exposed copper on areas not to be soldered is permitted on 1% of the conductor surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor edges.

3.6 Structural Integrity Printed boards **shall** meet structural integrity requirements for thermally stressed (after solder float) evaluation test coupons specified in 3.6.2.

Although the A and B or A/B coupons are assigned for this test, production boards may be used in lieu of the A and B or A/B coupons. Areas selected from boards **shall** contain holes and copper features so that all criteria within this specification can be evaluated. The production boards and all other test coupons in the quality conformance test circuitry which contain plated-through holes **shall** be capable of meeting the requirements of this section. Structural integrity **shall** be used to evaluate test coupons or production boards from Type 2 through Type 6 boards by microsectioning techniques. Characteristics not applicable to Type 2 boards (i.e., requirements for innerlayer separations, innerlayer inclusions, and inner foil cracks) are not evaluated. Dimensional measurements that are only possible through the use of microsectioning techniques are also defined in this section. Blind and buried vias **shall** meet the requirements of plated-through holes. Refer to IPC-2221 for appropriate coupon design of blind and buried vias for plated hole evaluation.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed test coupon and all requirements must be met; however, per supplier election, certain properties and conditions as defined in the following paragraph(s), which are not affected by thermal stressing, may be evaluated in a test coupon(s) that has not been thermally stressed.

a) When a supplier elects to evaluate the unstressed test coupon for the properties listed in (b), he may do so at any operation following the copper plating operation. If the board undergoes additional thermal excursions above the T_g (glass transition temperature) after copper plating, the unstressed test coupon being evaluated **shall** also be subjected to these thermal excursions.

b) The properties which are not affected by thermal stress include but are not limited to: copper voids, plating folds/inclusions, burrs and nodules, glass fiber protrusion, wicking, final coating plating voids, etchback, negative etchback, plating/coating thickness, internal and surface copper layer or foil thickness.

3.6.1 Thermal Stress Testing Test coupons or production boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.8.

Following stress, test coupons or production boards **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1, or 2.1.1.2 on test coupons or production boards. Evaluation of all applicable holes and vias, including blind and buried, for all such structures found on the finished printed board **shall** be inspected in the vertical cross section in accordance with Table 4-3. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the holes is within 10% of the drilled diameter of the hole.

Plated-through holes **shall** be examined for foil and plating integrity at a magnification of 100X ± 5%. Referee examinations **shall** be accomplished at a magnification of 200X ± 5%. Each side of the hole **shall** be examined independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination and plating voids, and so forth, **shall** be accomplished at magnifications specified above. For foils less than 3/8 oz., higher magnifications may be required to confirm minimum thickness requirement. Plating thicknesses below 1.0 µm [39.4 µin] **shall not** be measured using metallographic techniques.

Note: When agreed by user and supplier, alternate techniques may be used to supplement microsection evaluation.

3.6.2 Requirements for Microsectioned Coupons or Production Boards When examined in microsection, the test coupons or production boards **shall** meet the requirements of Table 3-6 and paragraph 3.6.2.1 through 3.6.2.17.

3.6.2.1 Plating Integrity Plating integrity in the plated-through holes **shall** meet the requirements detailed in Table 3-6. For Class 2 and 3 product, there **shall** be no separation of plating layers (except as noted in Table 3-6), no plating cracks, and internal interconnections **shall** exhibit no separation or contamination between plated hole wall and internal layers.

Metal core or thermal planes, when used as electrically functional circuitry, **shall** meet the above requirements when made from copper; but those made from dissimilar metals may have small spots or pits at their junction with the hole wall plating. Those areas of contamination or inclusions **shall** neither exceed 50% of each side of the interconnection, nor occur in the interface of the copper cladding on the core and the copper plating in the hole wall when viewed in the microsection evaluation.

3.6.2.2 Plating Voids Class 1 product **shall** meet the requirements for plating voids established in Table 3-6. For Class 2 and 3 product, there **shall** be no more than one void per test coupon or production board, and the following criteria must be met:

a. There **shall** be no more than one plating void per test coupon or production board, regardless of length or size.

b. There **shall** be no plating void in excess of 5 percent of the total printed wiring board thickness.

c. There **shall** be no plating voids evident at the interface of an internal conductive layer and plated hole wall.

d. Circumferential plating voids greater than 90° are not allowed.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated hole

Table 3-6 Plated Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper voids.	Three voids allowed per hole. Voids in the same plane are not allowed. No void **shall** be longer than 5% of board thickness. No circumferential voids greater than 90° allowed.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.
Plating folds/inclusions[2].	Must be enclosed.	Must be enclosed.	Must be enclosed.
Burrs and nodules[2].	Allowed if minimum hole diameter is met.	Allowed if minimum hole diameter is met.	Allowed if minimum hole diameter is met.
Glass fiber protrusion.	Allowed. See 3.6.2.11.	Allowed. See 3.6.2.11.	Allowed. See 3.6.2.11.
Wicking (Copper Plating).	125 µm [4,921 µin] maximum	100 µm [3,937 µin] maximum	80 µm [3,150 µin] maximum
Innerlayer inclusions (inclusions at the interface between internal lands and through hole plating).	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	None allowed.
Internal foil cracks[1].	"C" cracks allowed on only one side of hole provided it does not extend through foil thickness.	None allowed.	None allowed.
External foil cracks[1] (Type "A," "B" and "D" cracks).	"D" cracks not allowed. "A" and "B" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.
Barrel/Corner cracks[1] (type "E" and "F" cracks).	None allowed.	None allowed.	None allowed.
Innerlayer separation (separation at the interface between internal lands and through hole plating).	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	None allowed.
Separations along the vertical edge of the external land(s).	Allowed (see Figure 3-4) provided it does not extend beyond the vertical edge of the external copper foil.		
Plating separation.	Allowed at knee, maximum length 130 µm [5,118 µin].	None allowed.	None allowed.
Hole wall dielectric/plated barrel separation.	Acceptable provided dimensional and plating requirements are met.	Acceptable provided dimensional and plating requirements are met.	Acceptable provided dimensional and plating requirements are met.
Lifted lands after thermal stress or rework simulation.	Allowed provided the finished boards meet the visual criteria of 3.3.4.		

[1]Copper crack definition: See Figure 3-5
"A" crack=A crack in the external foil
"B" crack=A crack that does not completely break plating (minimum plating remains)
"C" crack=A crack in the internal foil
"D" crack=A crack in the external foil and plating-complete break in foil and plating
"E" crack=A barrel crack in plating only
"F" crack= A corner crack in the plating only
[2]The minimum copper thickness in Table 3-2 must be met.

exhibiting this condition **shall** be counted as having a single void for panel acceptance purposes.

If a void is detected during evaluation of a microsection which meets the above criteria, resample in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no plating voids, the product which the test coupon or production boards represent are considered acceptable; however, if a plating void is present in the microsections, the product **shall** be considered nonconforming.

3.6.2.3 Laminate Voids For Class 2 and 3 products, there **shall** be no laminate voids in Zone B (Figure 3-8) in excess of 80 µm [3,150 µin]. For Class 1 products, voids allowed in Zone B (Figure 3-8) **shall not** exceed 150 µm [5,906 µin]. Multiple voids between two adjacent plated-through holes in the same plane **shall not** have a combined length which exceeds these limits. Voids between two uncommon conductors in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.6.2.4 Laminate Cracks Laminate cracks in Zone A (Figure 3-8) are acceptable. Cracks that originate in Zone A and extend into Zone B or are entirely in Zone B **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or 3 products, and 150 µm [5,906 µin] for Class 1 products. Multiple cracks between two adjacent plated-through holes

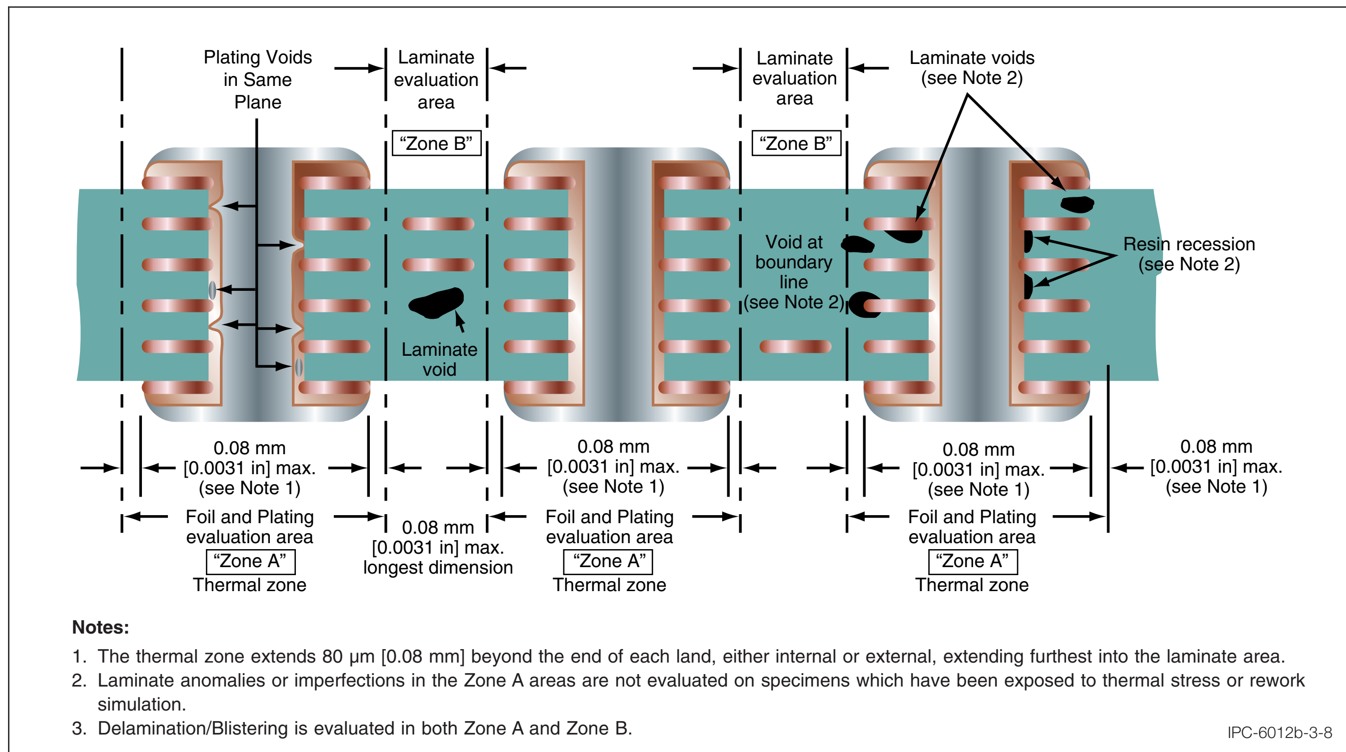

Figure 3-8 Typical Microsection Evaluation Specimen

in the same plane **shall not** have a combined length which exceeds these limits. Cracks between two uncommon conductors in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.6.2.5 Delamination or Blistering For Class 2 and 3 there **shall** be no evidence of delamination or blistering. For Class 1, if delamination or blistering is present, evaluate the entire board per 3.3.2.3.

3.6.2.6 Etchback When specified on the master drawing, printed boards **shall** be etched back for the lateral removal of resin and/or glass fibers from the drilled hole walls prior to plating. The etchback **shall** be between 5 µm [197 µin] and 80 µm [3,150 µin] with a preferred depth of 13 µm [512 µin]. Shadowing is permitted on one side of each land. When no etchback is specified and the board manufacturer elects to use etchback, the manufacturer **shall** be qualified to perform etchback through demonstration of qualification test coupons or boards. **Caution:** Etchback greater than 50 µm [1,969 µin] may cause folds or voids in the plating, which then may not meet the required copper thickness.

3.6.2.7 Smear Removal Smear removal is removal of resin debris that results from the formation of the hole. Smear removal **shall** be sufficient to meet the acceptability criteria for plating separation (see Table 3-6). Smear removal **shall not** be etched back greater than 25 µm [984 µin]; random tears or drill gouges which produce small areas where the 25 µm [984 µin] depth is exceeded **shall not** be evaluated as smear removal. Smear removal is not required of Type 1 or Type 2 boards.

3.6.2.8 Negative Etchback Negative etchback **shall not** exceed the requirements shown in Figure 3-9.

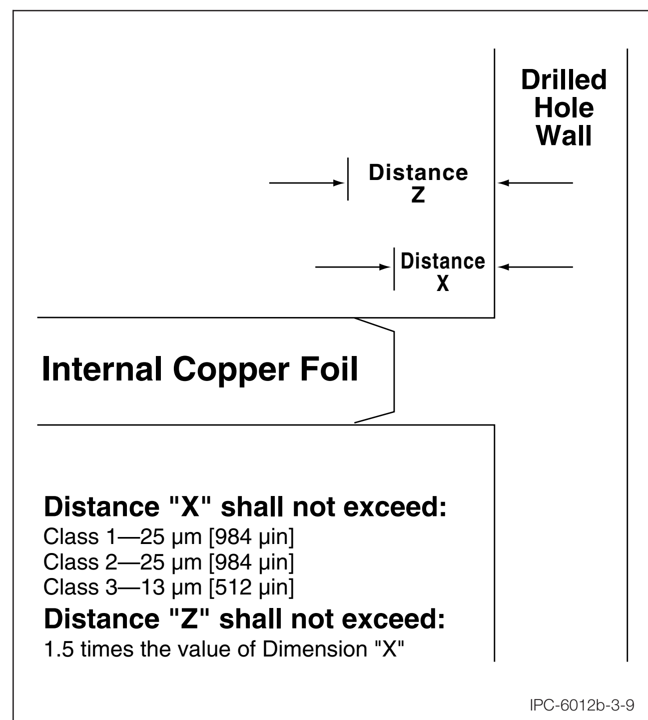

Figure 3-9 Negative Etchback

3.6.2.9 Annular Ring and Breakout (Internal) Internal annular ring, if not determined by alternate techniques as agreed upon between user and supplier **shall** be measured by microsection to verify conformance to Table 3-5 as shown in Figure 3-10. Measurements for internal annular ring are from the inside of the drilled hole to the edge of the internal land as shown in Figure 3-10. Negative etchback is evaluated per 3.6.2.8 and Figure 3-9. External pads of sequentially laminated structures are considered as an external layer and are evaluated in process prior to additional lamination(s) (see 3.4.2). Microsection analysis is performed per 3.6.2 (see Figures 3-2 and 3-3). Unless prohibited by the customer, the employment of filleting or ''tear drops'' to create additional land area at the conductor junction **shall** be acceptable for Class 1 and 2 and in accordance with general requirements for lands with holes detailed in IPC-2221. Employment of filleting or ''tear drops'' in Class 3 product **shall** be as agreed upon between user and supplier.

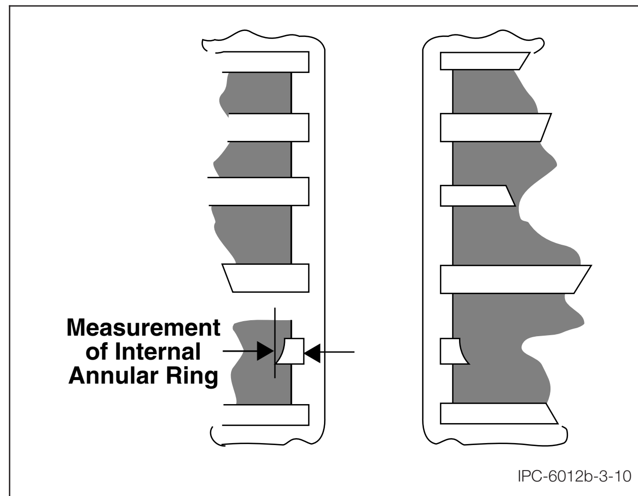

Figure 3-10 Annular Ring Measurement (Internal)

Note: Consideration should be given to how the microsection cut is ''clocked,'' or rotated. Misregistration can occur randomly as opposed to orthogonally and therefore an orthogonal cut will not guarantee that a microsection view will portray hole breakout, if it exists. See Figures 3-11 and 3-12 for an example of how breakout may or may not be detected within a microsection based on the rotation.

For Class 2 boards, if internal annular ring breakout is detected in the vertical cross section, but the degree of breakout cannot be determined, internal registration may be assessed by nondestructive techniques other than microsection, such as, special patterns, probes, and/or software, which are configured to provide information on the interpolated annular ring remaining and pattern skew. Techniques include, but are not limited to the following:

- The optional F coupon.
- Custom designed electrically testable coupons.

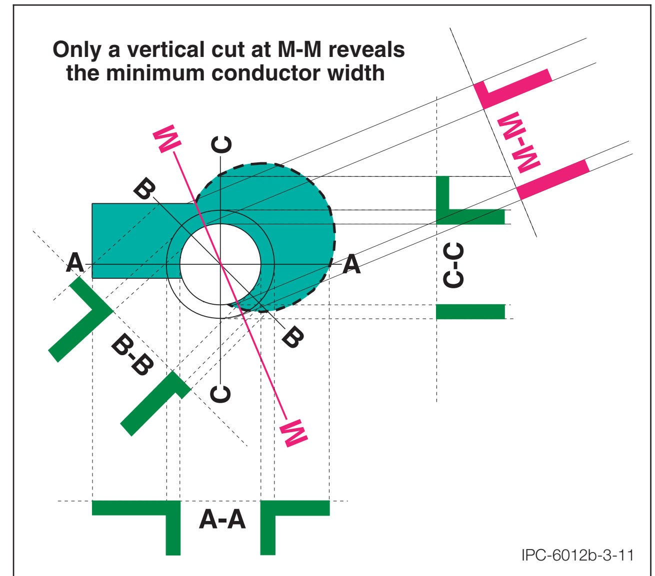

Figure 3-11 Microsection Rotations for Breakout Detection

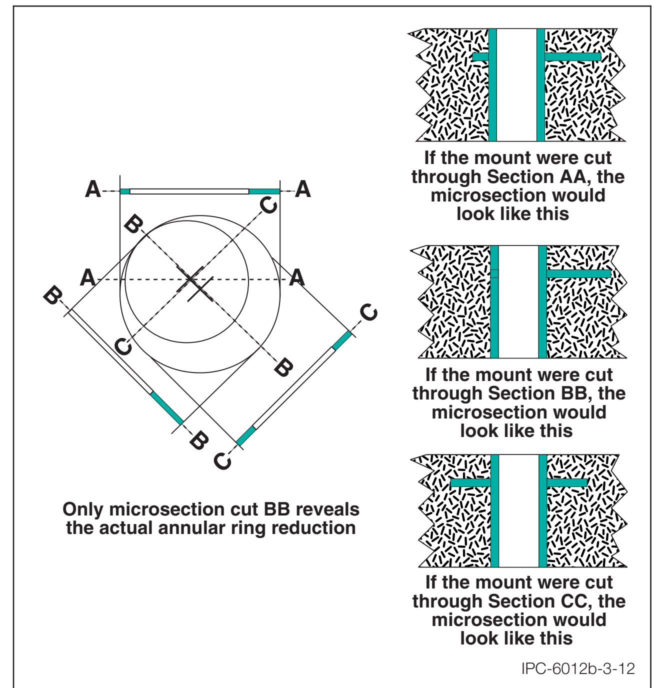

Figure 3-12 Comparison of Microsection Rotations

- Radiographic (x-ray) techniques.
- Horizontal microsection.
- CAD/CAM data analysis as correlated to pattern skew by layer.

Note: Microsectioning or statistical sampling **shall** be used to verify correlation of the approved technique, and a calibration standard established for the specific technique employed.

3.6.2.9.1 Breakout (Internal) Conditions If misregistration to the point of breakout is detected in vertical microsections, the concerns are that:

1. The conductor width minimum may be compromised at the land junction and,
2. There is insufficient electrical spacing.

The extent and direction of misregistration **shall** be determined.

Actual boards or appropriate test coupons **shall** then be tested to determine compliance. This may be accomplished by the techniques listed in 3.6.2.9.

3.6.2.10 Lifted Lands Lifted lands are allowed on the thermally stressed microsection.

3.6.2.11 Plating/Coating Thickness Based on microsection examination or on the use of suitable electronic measuring equipment, plating/coating thicknesses **shall** meet the requirements of Table 3-2, or as specified in the procurement document. Measurements in the plated-through hole **shall** be reported as an average thickness per side of the hole. Isolated thick or thin sections **shall not** be used for averaging. Isolated areas of reduced copper thickness due to glass fiber protrusions **shall** meet the minimum thickness requirements of Table 3-2 as measured from the end of the protrusion to the hole wall.

If copper thickness less than the minimum specified in Table 3-2 is detected in isolated areas, it should be considered a void and resample in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or production boards have no isolated areas of reduced copper thickness, the product which the test coupons or production boards represent are considered acceptable; however, if reduced copper thickness is present in the microsections, the product **shall** be considered nonconforming.

3.6.2.11.1 Copper Wrap Plating Copper wrap plating minimum as specified in Table 3-2 **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required (see Figures 3-13 and 3-14). Reduction of wrap-plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-15).

3.6.2.12 Minimum Internal Layer Copper Foil Thickness If the internal conductor thickness is specified by a foil weight, the minimum internal copper thickness after processing **shall** be in accordance with Table 3-7 for all classes. This table is based on minimum copper foil thickness allowances per IPC-4562 followed by two successive scrubbings. Each scrub is expected to remove a specific amount of copper and is represented in the table by a variable processing allowance reduction. When the procurement documentation specifies a minimum copper thickness for internal conductors, the conductor **shall** meet or exceed that minimum thickness.

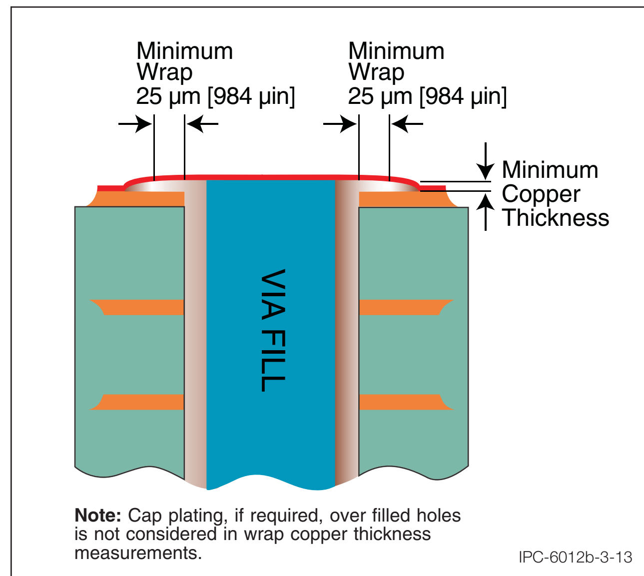

Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes)

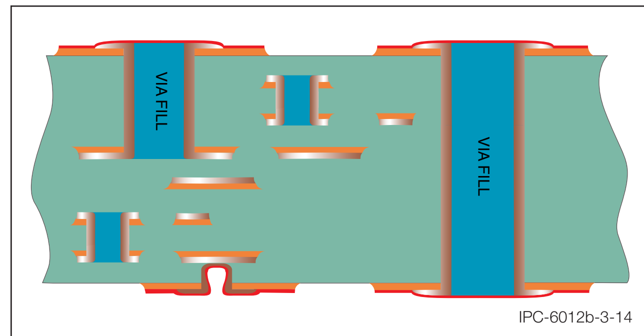

Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable)

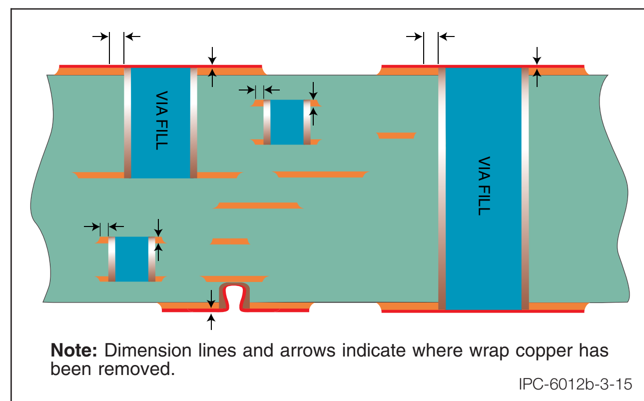

Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

3.6.2.13 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-8. When the procurement documentation specifies

Table 3-7 Internal Layer Foil Thickness after Processing

Weight	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Maximum Variable Processing Allowance Reduction* (µm) [µin]	Minimum Final Finish after Processing (µm) [µin]
1/8 oz. [5.10]	4.60 [181]	1.50 [59]	3.1 [122]
1/4 oz. [8.50]	7.70 [303]	1.50 [59]	6.2 [244]
3/8 oz. [12.00]	10.80 [425]	1.50 [59]	9.3 [366]
1/2 oz. [17.10]	15.40 [606]	4.00 [157]	11.4 [449]
1 oz. [34.30]	30.90 [1,217]	6.00 [236]	24.9 [980]
2 oz. [68.60]	61.70 [2,429]	6.00 [236]	55.7 [2,193]
3 oz. [102.90]	92.60 [3,646]	6.00 [236]	86.6 [3,409]
4 oz. [137.20]	123.50 [4,862]	6.00 [236]	117.5 [4,626]
Above 4 oz. [137.20]	IPC-4562 value less 10% reduction	6.00 [236]	6 µm [236 µin] below minimum thickness of calculated 10% reduction of foil thickness in IPC-4562

* Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.

Table 3-8 External Conductor Thickness after Plating

Weight[1]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm) [787 µin][2]	Plus minimum plating for Class 3 (25 µm) [984 µin][2]	Maximum Variable Processing Allowance Reduction[3] (µm) [µin]	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

1. Starting foil weight of design requirement per procurement documentation.
2. Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.
3. Reference: Min. Cu Plating Thickness
Class 1 = 20 µm [787 µin] Class 2 = 20 µm [787 µin] Class 3 = 25 µm [984 µin]

a minimum copper thickness for external conductors, the test coupon or production board **shall** meet or exceed that minimum thickness. The minimum surface conductor thickness after processing values given in Table 3-8 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c

Where:

a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).

b = Minimum copper plating thickness (20 µm [787 µin] for Class 1 and 2; 25 µm [984 µin] for Class 3).

c = A maximum variable processing allowance reduction.

3.6.2.14 Metal Cores The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or plated-through holes, and the metal plane **shall** be 100 µm [3,937 µin] (see Figure 3-16).

3.6.2.15 Dielectric Thickness The minimum dielectric spacing **shall** be specified in the procurement documenta-

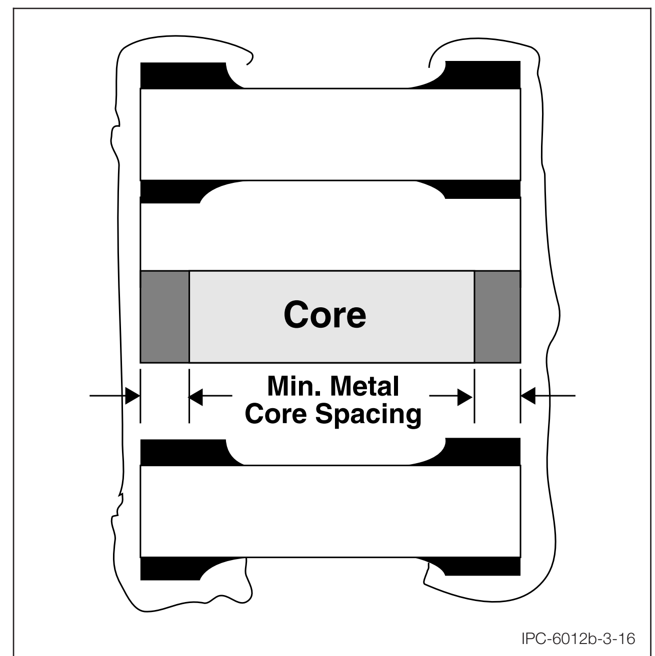

Figure 3-16 Metal Core to Plated-Through Hole Spacing

tion. Figure 3-17 provides an example of a measurement technique for minimum dielectric spacing.

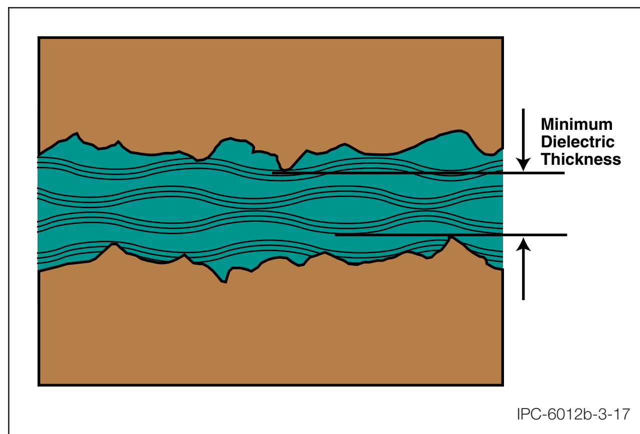

Figure 3-17 Measurement of Minimum Dielectric Spacing

Note: Minimum dielectric spacing may be specified to be 30 µm [1,181 µin]; however, low profile copper foils should be used and the voltages employed should be taken into consideration so as not to cause breakdown between layers. If the minimum dielectric spacing and the number of reinforcing layers are not specified, the minimum dielectric spacing is 90 µm [3,543 µin] and the number of reinforcing layers may be selected by the supplier. When the nominal dielectric thickness on the drawing is less than 90 µm [3,543 µin], the minimum dielectric spacing is 25 µm [984 µin] and the number of reinforcing layers may be selected by the supplier.

3.6.2.16 Material Fill of Blind and Buried Vias Fill requirements for blind vias **shall** be as specified in the procurement documentation. Buried vias **shall** be at least 60% filled with the laminating resin or similar via filling material for Class 2 and Class 3. They may be completely void of fill material for Class 1.

3.6.2.17 Nail Heading No evidence exists that nail heading affects functionality. The presence of nail heading may be considered an indicator of process or design variation but is not a cause for rejection.

3.7 Solder Resist (Solder Mask) Requirements When solder resist is required on printed boards, it **shall** meet the qualification/conformance requirements of IPC-SM-840. If a solder resist performance class is not specified for Class 1 or 2, IPC-SM-840 Class T **shall** be used. For Class 3 board performance, IPC-SM-840 Class H **shall** be used. The following other conformance requirements apply:

3.7.1 Solder Resist Coverage Solder resist coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

a. Metal conductors **shall not** be exposed in areas where solder resist is required. Touch up, if required to cover these areas with solder resist, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist.

b. In areas containing parallel conductors, solder resist variations **shall not** expose adjacent conductors unless the area between the conductors is purposely left blank as for a test point or for some surface mount devices.

c. Conductors under components **shall not** be exposed or **shall** be otherwise electrically isolated. If the component pattern is not readily apparent, the area covered by a component **shall** be shown in the procurement document.

d. Solder resist need not be flush with the surface of the land. Misregistration of a solder resist defined feature **shall not** expose adjacent isolated lands or conductors.

e. Solder resist is allowed on lands for plated-through holes to which solder connections are to be made provided the external annular ring requirements for that Class of products are not violated; resist **shall not** encroach upon the barrel of this type of plated-through hole. Other surfaces such as edge board connector fingers and surface mount lands **shall** be free of solder resist except as specified. Solder resist is allowed in plated-through holes and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled. Solder resist may tent or plug via holes and may be required for that purpose. Test points that are intended for assembly testing must be free of solder resist unless coverage is specified.

f. When a land contains no plated-through holes, as in the case of surface mount or ball grid array lands, misregistration **shall not** cause encroachment of the solder resist on the land or lack of solder-resist-definition in excess of the following:

   1) on surface mount lands misregistration **shall not** cause encroachment of the solder resist over the land area greater than 50 µm [1,969 µin] for a pitch of 1.25 mm [0.04921 in] or greater; and encroachment **shall not** exceed 25 µm [984 µin] for a pitch less than 1.25 mm [0.04921 in]; encroachment may occur on adjacent sides but not on opposite sides of a surface mount land.

   2) on ball grid array lands, if the land is solder-resist-defined, misregistration may allow a 90° breakout of the solder resist on the land; if clearance is specified, no encroachment of the solder resist on the land is allowed except at the conductor attachment.

g. Pits and voids are allowed in nonconductor areas provided they have adherent edges and do not exhibit lifting or blistering in excess of allowance in 3.7.2.

h. Coverage between closely spaced surface mount lands **shall** be as required by procurement documentation.

i. When design requires coverage to the board edge, chipping or lifting of solder resist along the board edge after fabrication **shall not** penetrate more than 1.25 mm [0.04921 in] or 50% of the distance to the closest conductor, whichever is less.

3.7.2 Solder Resist Cure and Adhesion The cured solder mask coating **shall not** exhibit tackiness, delamination, bubbles or blistering to the following extent:

- Class 1 does not bridge between conductors.
- Class 2 and 3 two per side, maximum size 0.25 mm [0.00984 in] in longest dimension, does not reduce electrical spacing between conductors by more than 25%.

Rework and touch up, if required to cover these areas with solder resist, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder resist. When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured solder resist lifting from the G coupon **shall** be in accordance with Table 3-9.

Table 3-9 Solder Resist Adhesion

	Maximum Percentage Loss Allowed		
Surface	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid- tin)	50	25	10

3.7.3 Solder Resist Thickness Solder resist thickness is not measured unless specified in the procurement documents. If a thickness measurement is required, instrumental methods may be used or assessment may be made using a microsection of the parallel conductors on the E coupon.

3.8 Electrical Requirements When tested as specified in Table 4-3 and Table 4-4, the printed boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.8.1 Dielectric Withstanding Voltage Applicable test coupons or production boards **shall** meet the requirements of Table 3-10, without flashover, or breakdown between conductors, or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

3.8.2 Electrical Continuity and Insulation Resistance Boards **shall** be tested in accordance with IPC-9252.

Table 3-10 Dielectric Withstanding Voltages

	Class 1	Class 2 and 3
Voltage For Spacing 80 µm [3,150 µin] or greater	No requirement	500 Vdc +15, -0
Voltage For Spacing less than 80 µm [3,150 µin]	No requirement	250 Vdc +15, -0
Time	No requirement	30 sec +3, -0

3.8.2.1 Continuity Printed boards and qualification test boards **shall** be tested in accordance with the procedure outlined below. There **shall** be no circuits whose resistance exceeds the values established in the procurement documentation. Specialized circuitry consisting of long runs of very narrow conductors, or short runs of very large conductors may increase or decrease these values. The acceptability criteria for these specialized conductors must be specified in the procurement documentation.

A current **shall** be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors **shall not** exceed that specified in IPC-2221 for the smallest conductor in the circuit. For qualification as referenced in 4.1.1 and 4.1.2, the test current **shall not** exceed one ampere. Boards with designed resistive patterns **shall** meet the resistance requirements specified on the master drawing.

3.8.2.2 Insulation Resistance Printed Boards or qualification test boards **shall** be tested in accordance with the following procedure. The insulation resistance between conductors **shall** meet the values established in the procurement documentation.

The voltage applied between networks must be high enough to provide sufficient current resolution for the measurement. At the same time, it must be low enough to prevent arc-over between adjacent networks, which could induce defects within the product. For manual testing, the voltage **shall** be 200 volts minimum and **shall** be applied for a minimum of five seconds. When automated test equipment is used, the minimum applied test voltage **shall** be the maximum rated voltage of the board. When not specified, use the default value in Table 1-2.

3.8.3 Circuit/Plated-Through Shorts to Metal Substrate Printed boards **shall** be tested in accordance with 3.8.1 except that polarizing voltage of 500 volts (DC) **shall** be applied between conductors and/or lands and the metallic heatsink in a manner such that each conductor/land area is tested (e.g., using a metallic brush or aluminum foil).

The board **shall** be capable of withstanding 500 volts (DC) between circuitry/plated-through holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

3.8.4 Moisture and Insulation Resistance (MIR) Test coupons **shall** be tested in accordance with the procedure outlined below. The test coupon **shall not** exhibit subsurface imperfections in excess of that allowed in 3.3.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-11 (at 500 volts DC). Noncomponent flush boards **shall** have a minimum requirement of 50 M for all classes. Insulation resistance requirements in the as-received condition are detailed in special requirement section (see 3.10.9).

Table 3-11 Insulation Resistance

	Class 1	Class 2	Class 3
As received	Maintain electrical function	500 MΩ	500 MΩ
After exposure to moisture	Maintain electrical function	100 MΩ	500 MΩ

The moisture and insulation resistance for printed boards **shall** be performed in accordance with IPC-TM-650, Method 2.6.3. Conformal coating in accordance with IPC-CC-830 **shall** be applied to the external conductors prior to chamber exposure. Final measurements **shall** be made at room temperature within two hours after removal from the test chamber. All layers have a 100 ± 10 volts DC polarizing voltage applied during chamber exposure. Mealing of the conformal coating **shall not** extend more than 3 mm [0.12 in] from the edge of the test coupon or production board.

3.8.4.1 Dielectric Withstanding Voltage After MIR A dielectric withstanding voltage test **shall** be performed after moisture and insulation resistance in accordance with 3.8.1.

3.9 Cleanliness Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.3.25 paragraph 4 Resistance of Solvent Extract Method. Equivalent methods may be used in lieu of the method specified; however it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified.

3.9.1 Cleanliness Prior to Solder Resist Application When a printed board requires a permanent solder resist coating, the uncoated boards **shall** be within the allowable limits of ionic and other contaminants prior to the application of solder resist coating. When noncoated printed boards are tested per 3.9, the contamination level **shall not** be greater than an equivalent of 1.56 $\mu g/cm^2$ of sodium chloride.

3.9.2 Cleanliness After Solder Resist, Solder, or Alternative Surface Coating Application When specified, printed boards **shall** be tested per 3.9 and meet the requirements in the procurement documentation.

3.9.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination When specified, inner layers **shall** be tested per 3.9 and meet the requirements of the procurement documentation.

3.10 Special Requirements When specified in the procurement documentation, some or all of the special requirements listed in this section (3.10) **shall** apply. A notation in the procurement documentation will designate which are required.

3.10.1 Outgassing The degree of outgassing **shall** have a Total Mass Loss (TML) of less than one percent (1%) and Collectible Volatile Condensable Material (CVCM) of less than one tenth of one percent (0.1%). Mass loss **shall** be determined on test coupons or production boards of representative substrates when tested in accordance with IPC-TM-650, Method 2.6.4.

3.10.2 Organic Contamination Noncoated printed boards **shall** be tested in accordance with the procedure outlined below. Any visual evidence of organic residue **shall** constitute a failure.

The printed board **shall** be tested in accordance with IPC-TM-650, Methods 2.3.38 or 2.3.39. The first is a qualitative method in which very pure acetonitrile is dripped across the test coupon or production board and collected on a microscope slide. It is dried and compared with a slide having dried, uncontaminated acetonitrile on it for visual evidence of organic residue. If evidence of organic contamination is detected by this test, Method 2.3.39 is used to determine the nature of the contaminant by the use of infrared spectrophotometric analysis using the Multiple Internal Reflectance (MIR) method.

3.10.3 Fungus Resistance Completed boards or representative board sections from the lot **shall not** support fungus growth when tested as follows: The specimen(s) **shall** be tested in accordance with IPC-TM-650, Method 2.6.1.

3.10.4 Vibration The test coupon or production board **shall** pass the circuitry test in 3.8.2 following the vibration test procedure below and **shall not** exhibit bow or twist in excess of that allowed in 3.4.4 following testing.

The boards **shall** be subjected to both a cycling and resonance dwell test with the flat surface of the board mounted perpendicular to the axis of vibration in accordance with IPC-TM-650, Method 2.6.9.

***Cycling Test* –** The cycling test **shall** consist of one sweep from 20 to 2000 Hz performed in 16 minutes. Input acceleration over the 20 to 2000 Hz frequency range **shall** be maintained to 15 Gs.

***Resonance Dwell* –** Test coupons or production boards **shall** be subjected to a 30 minute resonance dwell with 25

Gs input or a maximum of 100 Gs output measured at the geometric center of the test coupon or production board. The test coupons or production boards **shall** be restrained from movement by fixturing on all four sides.

3.10.5 Mechanical Shock The test boards **shall** pass the circuitry test in 3.8.2 after being subjected to mechanical shock testing as follows.

The mechanical shock test **shall** be performed in accordance with IPC-TM-650, Method 2.6.5. The boards **shall** be subjected three times to a shock pulse of 100 Gs with a duration of 6.5 milliseconds in each of the three principal planes. The test coupons or production boards **shall** be restrained from movement by fixturing on all four edges.

3.10.6 Impedance Testing Requirements for impedance **shall** be specified on the master drawing. Impedance testing may be performed on a test coupon or a designated circuit in the production board. Time Domain Reflectometers (TDR) are used for electrical testing, but for large impedance tolerances, mechanical measurements from a microsection utilizing a special test coupon can be used to calculate and verify impedance values. (See IPC-2251 for the equations for calculating impedance from the test coupon and IPC-TM-650, Method 2.5.5.7, for the test method using the TDR technique.)

3.10.7 Coefficient of Thermal Expansion (CTE) When boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the Coefficient of Thermal Expansion **shall** be within ± 2 ppm/°C for the CTE and temperature range specified on the procurement documentation. Testing **shall** be by the strain gauge method in accordance with IPC-TM-650, Method 2.4.41.2. If agreed upon by user and supplier, other methods of determining the CTE may be used.

3.10.8 Thermal Shock When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.6.7.2. An increase in resistance of 10% or more **shall** be considered a reject. After microsectioning, the boards or test coupons **shall** meet the requirements of Table 3-6 and Figure 3-5.

3.10.9 Surface Insulation Resistance (As Received) Test coupons **shall** be tested in accordance with the procedure outlined below. The insulation resistance **shall** be no less than that shown in Table 3-11.

Test coupons or production boards should be conditioned at 50 ± 5 °C [122 ± 9 °F] with no added humidity for a period of 24 hours. After cooling, the insulation resistance test **shall** be performed in accordance with the ambient temperature measurements specified in IPC-TM-650, Method 2.6.3.

3.10.10 Metal Core (Horizontal Microsection) When specified, metal core printed boards which have clearance between the plated-through holes and the metal core **shall** require a horizontal microsection prepared to view the metal core/hole fill insulation. Test coupons or production boards **shall** have been subjected to thermal stress in accordance with 3.6.1 prior to microsectioning. Wicking, radial cracks, lateral spacing or voids in the hole-fill insulation material **shall not** reduce the electrical spacing between adjacent conductive surfaces to less than 100 µm [3,937 µin]. Wicking and/or radial cracks **shall not** exceed 75 µm [2,953 µin] from the plated-through hole edge into the hole-fill.

3.10.11 Rework Simulation

3.10.11.1 Through Hole Components When specified, printed boards or test coupons **shall** be tested in accordance with IPC-TM-650, Method 2.4.36 and then microsectioned and examined in accordance with 3.6. Lifted lands are allowed.

3.10.11.2 Surface Mount Components When specified, 100% surface mount boards **shall** be tested in accordance with the procurement documentation.

3.10.12 Bond Strength, Unsupported Component Hole Land The unsupported component hole lands **shall** be tested in accordance with IPC-TM-650, Method 2.4.21. The unsupported component hole land **shall** withstand 2 kg or 35 kg/cm^2, whichever is less.

Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.11 Repair Repair of bare boards **shall** be as agreed upon between the user and supplier for each set of procurement documentation (see IPC-7711/21A).

3.11.1 Circuit Repairs When agreed on between user and supplier, circuit repairs on Classes 1, 2, and 3 will be permitted. As a guideline, there should be no more than two circuit repairs for each 0.09 m^2 or less of layer area per side. Circuit repairs on any impedance controlled circuits **shall not** violate the impedance requirement and **shall** have the agreement of the user. Circuit repairs **shall not** violate the minimum electrical spacing requirements.

3.12 Rework Rework is permitted for all Classes. The touch-up of surface imperfections in the base material or removal of residual plating materials or extraneous copper will be permitted for all products when such action does not affect the functional integrity of the board.

4 QUALITY ASSURANCE PROVISIONS

4.1 General General Quality Assurance Provisions are specified in IPC-6011 and each sectional specification. The

requirements specific to Rigid Boards are contained in this specification and include the Qualification Testing, Acceptance Testing and Frequency of Quality Conformance Testing.

4.1.1 Qualification Qualification is agreed upon by the user and supplier (see IPC-6011). The qualification should consist of capability analysis assessments (see IPC-9151), preproduction samples, production sample or test coupons (see IPC-6011) that are produced by the same equipment and procedures planned for the production boards. Qualification should include those applicable tests as referenced in Tables 4-3 and 4-4. Qualification as agreed by the user may consist of documentation that supplier has furnished similar product to other users or to other similar specifications.

4.1.2 Sample Test Coupons Sample test coupons may be used for qualification or for on-going process control. Master drawings, databases, or phototools are available from IPC. For each type (see 1.3.2) the master drawing and phototool is listed as follows:

Type 1 Use surface layers of IPC-A-47
Type 2 Use surface layers of IPC-A-47
Type 3 Use Master Drawing IPC-100103 within IPC-A-47

Note: IPC-100002 is the universal drilling and profile master drawing. Both the IPC-100103 and IPC-100002 are part of the IPC-A-47 phototool artwork package.

Table 4-1 specifies the test coupons on the sample used for qualification and process capability evaluations. The numerical designation following each coupon, such as M5, relates to multiple instances of the coupon on the sample as indicated within IPC-A-47.

4.2 Acceptance Tests Use the C=0 Zero Acceptance Number Sampling Plan specified in Table 4-2 when ''Sample'' is indicated in Table 4-3. Acceptance testing **shall** be performed as specified in Table 4-3 to the requirements of this specification and IPC-6011 using either test coupons and/or production boards. The test coupons are described in IPC-2221, which indicates the purpose of each coupon and its frequency on a manufacturing panel.

4.2.1 C=0 Zero Acceptance Number Sampling Plan The C=0 Zero Acceptance Number Sampling Plan provides greater or equal protection for the Lot Tolerance Percent Defective (L.T.P.D.) protection at the 0.10 ''consumer risk'' level. The Index Values at the top of each sample size column associates to the A.Q.L. level. For a lot to be accepted, all samples (shown in Table 4-2) **shall** conform to the requirements. Disposition of rejected lots **shall** be fully documented. Contact the American Society for Quality Control for more information on sampling plans (H0862).

4.2.2 Referee Tests Two additional microsection sets from the same panel may be prepared and evaluated for microsection defects that are considered to be isolated or random in nature or caused by microsection preparation. For acceptance, both referee sets must be defect free.

4.3 Quality Conformance Testing Quality Conformance Testing **shall** consist of inspections specified in Table 4-4 in a laboratory, which meets all requirements of IPC-QL-653, unless otherwise specified by the user. Class 3 testing may be extended to reliability test and evaluation for Class 2.

4.3.1 Coupon Selection Two sets of test coupons of the most complex pattern of each type of material processed during the inspection period **shall** be selected from lots that have passed acceptance testing.

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,5	Types 4, 6	Board
Visual (1)	All	All	All	X
Solderability				
Surface (1)	M2, M5			
Hole (1)		S1, S6	S1, S6	
Dimensional (1)	All	All	All	X
Physical				
Plating Adhesion (1)	N1, N4, N5	N1, N4, N5	N1, N4, N5	
Bond Strength	A2, A3, A6			
Construction Integrity				
PTH Prior to Stress		A1, A4, A5	Design Req.	
Additional Dimensions		A1, A4, A5	Design Req.	
PTH After Stress				
Thermal Stress		A1, A4, A5	Design Req.	
Horizontal micro (Metal Core)		B1, B4, B5	A1, B4, B5	
Rework Simulation		B2, B3, B6	Design Req.	
Electrical Requirements				
DWV	E1, E4, E5	E1, E4, E5	E1, E4, E5	
Continuity	D1, D4, D5	D1, D4, D5	Design Req.	
Insulation Resistance	E2, E3, E6	E2, E3, E6	E2, E3, E6	
Environmental				
Thermal Shock	D2, D3, D6	D2, D3, D6	Design Req.	
Cleanliness (1)				X
Moisture/Insulation Resistance	E1, E4, E5	E1, E4, E5	E1, E4, E5	
Special Requirements (2)				
Outgassing				X
Organic Contamination				X
Fungus				X
Vibration				X
Mechanical Shock				
Impedance		H1, H2, H3		
Thermal Expansion				

Note 1 – Not technology dependent.
Note 2 – Additional test coupons required, to be agreed upon between user and manufacturer.

Table 4-2 C=0 Sampling Plan (Sample Size for Specific Index Value*)

	Class 1			Class 2			Class 3			
Lot Size	2.5*	4.0*	6.5*	1.5*	2.5*	4.0*	0.10*	1.0*	2.5*	4.0*
1-8	5	3	2	**	5	3	**	**	5	3
9-15	5	3	2	8	5	3	**	13	5	3
16-25	5	3	3	8	5	3	**	13	5	3
26-50	5	5	5	8	5	5	**	13	5	5
51-90	7	6	5	8	7	6	**	13	7	6
91-150	11	7	6	12	11	7	125	13	11	7
151-280	13	10	7	19	13	10	125	20	13	10
281-500	16	11	9	21	16	11	125	29	16	11
501-1200	19	15	11	27	19	15	125	34	19	15
1201-3200	23	18	13	35	23	18	125	42	23	18
3201-10,000	29	22	15	38	29	22	192	50	29	22
10,001-35,000	35	29	15	46	35	29	294	60	35	29

*Index Value is associated to the A.Q.L. value. If a particular product is determined to be "critical" by the user and a smaller index value is required, the user **shall** designate the requirement in the procurement document and should state the "critical" requirement on the master drawing.
**Denotes inspect entire lot.

Table 4-3 Acceptance Testing and Frequency

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Production Board	Test Coupon By Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Material	3.2.1-3.2.14			Manufacturer's Certification			Verifiable certificate of compliance or SPC program
Visual							
Edges of board	3.3.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Laminate imperfections	3.3.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Voids in plated hole	3.3.3	X		Sample (4.0)	Sample (2.5)	Sample (1.0)	Per panel
Lifted lands	3.3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Marking and traceability	3.3.5	X	Coupons and board	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Workmanship	3.3.9	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solderability							
Surface	3.3.6		M	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Hole[7]	3.3.6		A or A/B or S	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Dimensional							
Board dimensional	3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Hole size	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Hole pattern accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Supplier certification allowed
Pattern feature accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Supplier certification allowed
Annular ring (external)	3.4.2	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Bow and twist	3.4.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Solder resist coverage	3.7-3.7.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per board
Plating/coating thickness (electronic)	3.6.2.11	X	C or N	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel[2]
Conductor Width							
Internal	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per internal panel layer
External	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Conductor Spacing							
Internal	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel layer (minimum 5 evaluations per layer set)
External	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per board
Conductive Surfaces (Surface Only)							
Edge board contact, junction of gold plate to solder finish	3.3.8	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Production Board	Test Coupon By Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Nicks, dents, pinholes	3.5.4.1	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Dewetting/ nonwetting/ final finish coverage	3.5.4.5 3.5.4.6 3.5.4.7	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Edge board connector	3.5.4.4	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per board
Surface mount	3.5.4.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Minimum 10 evaluations per panel
Physical							
Plating adhesion	3.3.7	X	C or N	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Solder resist cure and adhesion	3.7 3.7.2	X	G	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Structural Integrity After Stress Types 3-6 (Microsection)[3]							
Plating integrity	3.6.2.1		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Laminate voids	3.6.2.3		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Etchback/ negative etchback	3.6 a & b 3.6.2.6 3.6.2.8		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Annular ring (internal)	3.6 a & b 3.6.2.9		A and B or 2 A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Twice per panel opposite corners[4,5]
Lifted lands	3.6.2.10		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Hole plating thickness	3.6 a & b 3.6.2.11		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Surface plating and conductor thickness	3.6 a & b 3.6.2.11 3.6.2.13		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Conductor thickness (internal)	3.6 a & b 3.6.2.12		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Metal core spacing	3.6.2.14		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Dielectric thickness	3.6 a & b 3.6.2.15		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Resin fill of buried vias	3.6.2.16		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Structural Integrity After Stress Type 2 (Microsection)[8]							
Plating integrity	3.6.2.1		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Laminate voids	3.6 a & b 3.6.2.3		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Lifted lands	3.6.2.10		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Hole plating thickness	3.6 a & b 3.6.2.11		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Surface plating and conductor thickness	3.6 a & b 3.6.2.11 3.6.2.13		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel

Inspection	Requirement and Method Section	Sample		Test Frequency						
		Production Board	Test Coupon By Board	Class 1[1]		Class 2[1]		Class 3[1]		Remarks
Electrical										
Circuit continuity	3.8.2.1	X		Type 1-2[6]	Type 3-6 Sample (2.5)	Type 1-2[6]	Type 3-6 100%	Type 1-2[6]	Type 3-6 100%	Per board
Insulation resistance	3.8.2.2	X		Type 1-2[6]	Type 3-6 Sample (2.5)	Type 1-2[6]	Type 3-6 100%	Type 1-2[6]	Type 3-6 100%	Per board
Cleanliness										
Cleanliness prior to solder resist application	3.9.1	X		Sample (6.5)		Sample (4.0)		Sample (4.0)		Per lot
Special Requirements (when specified)										
Metal core (horizontal microsection)	3.10.10	As specified by contract or master drawing								
Solder resist thickness	3.7.3									
Dielectric withstanding voltage	3.8.1									
Circuit/plated though shorts to metal substrate	3.8.3									
Cleanliness after surface coating application	3.9.2									
Cleanliness of inner layers after oxide treatment prior to lamination	3.9.3									
Outgassing	3.10.1									
Organic contamination	3.10.2									
Fungus resistance	3.10.3									
Vibration	3.10.4									
Mechanical shock	3.10.5									
Impedance testing	3.10.6									
Coefficient of thermal expansion	3.10.7									
Thermal shock	3.10.8									
Surface insulation resistance (as received)	3.10.9									
Repair	3.11									
Circuit repair	3.11.1									

Notes:
1. Number in parentheses is the AQL level.
2. Measurment location must be larger than collimated source.
3. All via structures **shall** be represented in the thermally stressed evaluations.
4. For Class 2 end product, the degree of breakout may be assessed by methods other than horizontal microsection.
5. The A and B or 2 A/B test coupons **shall** be taken from opposite corners of the manufacturing panel and in opposing axes (one in the "x" axis and the other in the "y" axis).
6. For Type 1 and 2 boards, visual or AOI inspection may be used in lieu of electrical testing.
7. Hole solderability testing not required for Type 2 double-sided boards without plated-through holes.
8. Cross sectioning not required for Type 2 double-sided boards without plated-through holes for plated-through hole evaluation.

Table 4-4 Quality Conformance Testing

Inspection	Requirement and Method Section	Test Coupon		Test Frequency		
		Type 1	Types 2-6	Class 1	Class 2	Class 3
Rework simulation (when specified)	3.10.11	-	A[1] or A/B[1]	NA	NA	Monthly
Bond strength	3.10.12	B or A/B	-	NA	Quarterly	Monthly
Dielectric withstanding voltage	3.8.1	E	E	NA	Quarterly	Monthly
Moisture and insulation resistance	3.8.4	E	E	NA	Quarterly	Monthly

[1]Test Coupon A or A/B contains the largest component hole and land associated with that hole that can be fitted to a 2.5 mm [0.0984 in] grid.

5 NOTES

5.1 Ordering Data The procurement documentation should specify the following:

A. Title, number, issue, revision letter, and date of current applicable master drawing.

B. Specific exceptions, variations, additions or conditions to this specification that are required by the user.

C. Part Identification and Marking instructions.

D. Information for preparation for delivery, if applicable.

E. Special tests required and frequency.

5.2 Superseded Specifications This specification supersedes and replaces IPC-6012B in the performance and requirements section.

IPC-6012B Performance Specification Sheet for Space and Military Avionics

This specification sheet lists common exceptions to existing IPC-6012B Class 3 performance attributes for use by the aerospace and military avionics sector of the electronics interconnect industry. These requirements are reflective of existing performance attributes within internal OEM industry specifications. They are listed here so that procurement documentation can easily specify requirements selected from within this specification sheet. Exceptions to IPC-6012B Class 3 performance attributes within this specification sheet are classified as Class 3/A requirements.

Requirement Attribute	IPC-6012B Section	Class 3/A Exception Requirement	Inspection/ Test Method	Conformance per Coupon or per Board	Remarks
Requirements	3		–	–	
Material	3.2	Type E3 (HTE) Copper	–	–	Certificate of Compliance
Copper Deposition	3.2.6.8	Tensile 40,000 PSI [275.8 MPa] or higher. Elongation 18% minimum			Performed Monthly
Visual	3.3		–	Per Board	
Profile	N/A		Visual		
Edges - Rigid Board	3.3.1		Visual		
Construction Imperfections	3.3.2		IPC-A-600		
Blistering, Delamination, Measling, Crazing, Haloing	3.3.2.1 - 3.3.2.3	No Delamination, blistering, measling or crazing allowed	IPC-A-600 Microsection or External Visual Examination		
Foreign Inclusions	3.3.2.4	No foreign inclusions allowed that reduce dielectric spacing below minimum	IPC-A-600		
Weave	3.3.2.5	No weave exposure allowed	Visual		
Scratches, Dents, Toolmarks	3.3.2.6		Visual		
Surface Microvoids	3.3.2.7		Visual		
Color Variations	3.3.2.8		Visual		
Pink Ring	3.2.2.9	Pink ring is acceptable as long as it does not reduce annular ring less than 0.05 mm [0.002 in] and does not increase with thermal stress			
Soldermask and Cover Coat Requirements	3.7		IPC-SM-840		
Soldermask and Cover Coat Coverage	3.7.1		Visual		
Soldermask and Cover Coat Cure and Adhesion	3.7.2		IPC-TM-650 Method 2.4.28.1	Per Panel	1 - G Coupon
Soldermask and Cover Coat Thickness	3.7.3	Solder Mask thickness 0.1 mm [0.004 in] max over laminate	Measurement or microsection	Per Panel	1 - E Coupon
Wicking/Plating Penetration	N/A		Visual	Per Board	
Plating and Finish Coating Voids in Hole	3.3.3	Hole - Class 3 Surface - None allowed	Visual	Per Board	
Marking	3.3.5		–	Per Board	
Solderability	3.3.6		J-STD-003		1 EA - C & A Coupon

Requirement Attribute	IPC-6012B Section	Class 3/A Exception Requirement	Inspection/ Test Method	Conformance per Coupon or per Board	Remarks
Solderability - Surface	3.3.6	8 hour steam surface Mount only per J-STD-003	IPC-J-STD-003	Per Panel	1 EA - C Coupon
Solderability - Plated-Through Hole	3.3.6		–		
Plating Adhesion	3.3.7		IPC-TM-650 Method 2.4.1	Per Panel	1 - C Coupon
Edge Board Contacts	3.3.8		Measurement	Per Board	
Lifted Lands	3.3.4		Visual	Per Board	
Workmanship	3.3.9		Visual	Per Board	
Dimensional	3.4		–	–	
Hole Size and Hole Pattern Accuracy	3.4.1		Measurement	Per Board	
Annular Ring	3.6.2.9 3.4.2	Unsupported holes - 0.38 mm [0.015 in] minimum Internal/External Plated-Through Holes - 0.051 mm [0.002 in] minimum allow 20% reduction unless already at 0.051 mm [0.002 in]	Visual or Microsection	Per Panel	4 - F Coupons (Optional)
Solderable Annular Ring (External)	N/A		Measurement	Per Board	
Bow and Twist	3.4.3	0.5%	IPC-TM-650 Method 2.4.22	Per Board	
Conductor Definition	3.5		IPC-A-600	Per Board	
Conductor Imperfections	3.5.3				
Conductor Width Reduction	3.5.3.1				
Conductor Thickness Reduction	3.5.3.2				
Conductor Spacing	3.5.2				
Conductive Surfaces	3.5.4		Measurement	Per Board	
Nicks, Dents and Pinholes	3.5.4.1				
Surface Mount Lands	3.5.4.2			Per Board	
Edge Connector Lands	3.5.4.4				
Dewetting	3.5.4.5	None allowed on surfaces to be soldered, including surface mount pads			
Nonwetting	3.5.4.6				
Final Finish Coverage	3.5.4.7				
Conductor Edge Outgrowth	N/A				
Structural Integrity before Thermal Stress	3.6	If nonstressed coupon is evaluated, it **shall not** have: Lifted lands, resin recession greater than 0.076 mm [0.003 in] depth or more than 40% of cumulative dielectric thickness, or laminate voids over 0.076 mm [0.003 in]	Microsection	Per Panel	1 - A or B Coupon
Structural Integrity after Thermal Stress	3.6		Microsection	Per Panel	1 - A or B Coupon

Requirement Attribute	IPC-6012B Section	Class 3/A Exception Requirement	Inspection/ Test Method	Conformance per Coupon or per Board	Remarks
Thermal Stress Testing	3.6.1			Per Panel	1 - A or B Coupon
Requirements for Microsectioned Coupons	3.6.2				
Laminate Integrity	3.6.2.3	No delamination or blistering, etc.	Microsection or External Visual Examination		
Laminate Voids	3.6.2.3				
Laminate Voids - Rigid	3.6.2.3				
Laminate Integrity - Cracks - Rigid	3.6.2.4	External laminate cracks not allowed			
Etchback	3.6.2.6	0.0051 mm [0.0002 in] - 0.04 mm [0.0015 in] When Required			
Smear Removal	3.6.2.7				
Negative Etchback	3.6.2.8	Not acceptable			
Plating Integrity (Space)	3.6.2.1	On metal core boards with dissimilar metals, contamination at the conductive interface **shall not** exceed 20%. No contamination can occur at copper foil interface			
Plating Integrity (Aerospace)	3.6.2.1	On metal core boards with dissimilar metals, contamination at the conductive interface **shall not** exceed 50%. No contamination can occur at copper foil interface			
Copper Voids	Table 3-6				
Plating Folds/Inclusions	Table 3-6				
Burrs and Nodules	Table 3-6				
Glass fiber Protrusion	Table 3-6				
Wicking	Table 3-6	50 µm [1,969 µin]			
Inner layer inclusions	Table 3-6				
Internal Foil Cracks	Table 3-6				
External foil Cracks (Types A, B and D)	Table 3-6				
Barrel/corner Cracks (Types E and F)	Table 3-6				
Innerlayer Separations	Table 3-6				
Separation Along Vertical Edge of External Lands	Table 3-6	Not acceptable			
Plating Separation	Table 3-6 3.6.2.1	Acceptable on 20% of Invar on CIC layers			
Hole wall dielectric/barrel separation	Table 3-6				
Lifted Lands after Stress or Rework	Table 3-6	Thickness of foil			
Plating Voids	3.6.2.2	No plating voids are allowed, isolated thin areas are allowed per 3.6.2.2			

Requirement Attribute	IPC-6012B Section	Class 3/A Exception Requirement	Inspection/ Test Method	Conformance per Coupon or per Board	Remarks
Plating/Coating Thickness	3.6.2.11	Via core/Buried vias 0.02 mm [0.0008 in] minimum Plated-Through Hole 0.04 mm [0.0015 in], minimum absolute 0.03 mm [0.0012 in] Low aspect ratio blind vias at 0.02 mm [0.0008 in] min			
Minimum Internal Layer Copper Foil Thickness	3.6.2.12				
Minimum Surface Conductor Thickness	3.6.2.13				
Metal Cores	3.6.2.14				
Dielectric Thickness	3.6.2.15	0.089 mm [0.0035 in] minimum with 2 layers prepreg if not specified on drawing			
Resin Fill of Blind and Buried Vias	3.6.2.16	Buried Vias: Buried vias completely filled; exceptions treated and evaluated as resin voids. Blind Vias: Minimum 75% fill			
Rework Simulation	3.10.11	Buried Vias: Buried vias completely filled; exceptions treated and evaluated as resin voids. Blind Vias: Minimum 75% fill	IPC-TM-650 Method 2.4.36	Per Panel	1 - B Coupon + 2 Coupons Per Month - Each Lot
Bond Strength - Unsupported Hole Land (Rigid Board)	3.10.12		IPC-TM-650 Method 2.4.21	Per Panel	1 - B Coupon + 2 Coupons Per Month - Each Lot
Electrical Requirements	3.8			–	
Dielectric Withstanding Voltage	3.8.1 & 3.8.4.1		IPC-TM-650 Method 2.5.7	Per Panel	1 - E Coupon + 2 E Coupons Per Month - Each Lot
Circuitry	3.8.2	Net List Testing - 250 Vdc - 100 Megohms Min		Per Board	
Continuity	3.8.2.1	Net List Testing - 250 Vdc - 10 Ohms Max	IPC-9252 & IPC-2221	Per Board	
Insulation Resistance	3.8.2.2	Net List Testing - 250 Vdc - 100 Megohms Min	IPC-9252	Per Board	
Insulation Resistance (As Received)	3.10.9	Net List Testing - 250 Vdc-100 Megohms Min	IPC-TM-650 Method 2.6.3	Per Board	1 - E Coupon
Environmental	N/A		–	–	
Moisture and Insulation Resistance	3.8.4		IPC-TM-650 Method 2.6.3	Per Panel	1 - E Coupon + 2 Coupons Per Month - Each Lot
Thermal Shock	3.10.8		IPC-TM-650	Per Panel	
Cleanliness	3.9 and 3.9.3	Ionic contamination testing required on finished board	IPC-TM-650 Method 2.3.25	Per Board	
Outgassing	3.10.1	All materials used in board			
Organic Contamination	3.10.2		IPC-TM-650 Method 2.3.38 or Method 2.3.39	Per Board	

Requirement Attribute	IPC-6012B Section	Class 3/A Exception Requirement	Inspection/ Test Method	Conformance per Coupon or per Board	Remarks
Fungus Resistance	3.10.3		IPC-TM-650 Method 2.6.1	Per Board	
Repair	3.11	No repair			
Solder Thickness	3.2.6 & Table 3-2	Minimum 3.8 µm [150 µin] (Electroplated Tin-Lead prior to fusing/reflow)			
Through Via Plugging		No plugged Through Hole or PTH Through Vias must meet same criteria as other Plated-Through Holes			
Microsection		Both X and Y (outside corner) and center of panel if multiple up			

APPENDIX A

Appendix A presents the performance requirements of IPC-6012B in an abbreviated form and alphabetical order. Special conditions, lengthy requirements, and tutorial information may be shortened or partially omitted in this appendix. See the referenced paragraph in this appendix for the full specification requirements.

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Etched Annular Ring (External Plated-Through Holes)	Not greater than 180° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed.	The minimum annular ring **shall** be 50 µm [1.969 µin].	3.4.2 and Table 3-5
Etched Annular Ring (External Unsupported Holes)	Not greater than 90° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed.	The minimum annular ring **shall** be 150 µm [5,906 µin].	3.4.2 and Table 3-5
Etched Annular Ring (Internal Plated-Through Holes)	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	The minimum internal annular ring **shall** be 25 µm [984 µin].	3.6.2.9 and Table 3-5
Bow and Twist	Maximum of 0.75% for surface mount boards and 1.5% for all other board technologies.			3.4.3
Burrs and Nodules	Allowed if minimum hole diameter is met.			3.6.2.1 and Table 3-6
Circuit Repair	No more than two repairs for each 0.09 m^2 [0.969 ft^2]; no impedance or minimum electrical spacing req. violated.			3.11.1
Circuitry	Testing conducted in accordance with IPC-9252.			3.8.2
Circuits/Plated-Through Hole Shorts to Metal Substrates	Metal core printed board **shall** withstand 500 volts DC between circuitry/plated-through holes and metal core substrates w/o flashover or dielectric breakdown.			3.8.3
Cleanliness	Testing in accordance to IPC-TM-650, Method 2.3.25, with contamination level of >1.56 µg/cm^2 of sodium chloride.			3.9.1
Coefficient of Thermal Expansion	If have metal cores/reinforcements with a req. to constrain thermal expansion in planar directions, CTE **shall** be within ± 2 ppm/°C for CTE and temp range spec on master drawing; testing w/ strain gauge method, according to IPC-TM-650, Method 2.4.41.2, unless otherwise agreed by user and supplier.			3.10.7
Color Variations in Bond Enhancement Treatment	Mottled appearance/color variation accept; Random missing areas of treatment **shall not** be >10%.			3.3.2.8
Conductor Definition	Meet visual and dimension req., pattern and thickness as specified in procurement documentation.			3.5
Conductor Imperfections	30% of minimum specified in 10% of length or 25 mm [0.984 in], whichever is less.	20% of minimum specified in 10% of length or 13 mm [0.512 in], whichever is less.		3.5.3
	No cracks, splits or tears.			
Conductor Spacing	Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced an additional 30% due to conductor edge roughness, spikes, etc., if not specified.		Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced <20% if not specified.	3.5.2
Conductor Surfaces				3.5.4
Conductor Thickness	If not specified, minimum conductor thickness **shall** be in accordance with 3.6.2.12 and 3.6.2.13.			3.5.1
Conductor Thickness Reduction	Reduction of conductor thickness not >30% of minimum.	Reduction of conductor thickness not >20% of minimum.		3.5.3.2
Conductor Width	If not specified, minimum conductor width **shall** be 80% of conductor pattern furnished.			3.5.1

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Conductor Width Reduction	Reduction of conductor width not >30% of minimum.	Reduction of conductor width not >20% of minimum.		3.5.3.1
Construction Imperfections	Measling, crazing, blistering and delamination.			3.3.2
Continuity	No circuits with resistance > the values established in the procurement documentation; current passed through for evaluation will not be > values in IPC-2221 for smallest conductor of circuit.			3.8.2.1
Copper Purity Elongation and Tensile Strength	Purity **shall** be no less than 99.5% pure, tensile strength not less than 36,000 PSI [248 MPa], elongation not less than 12%.			3.2.6.8
Cracks, Barrel/Corner	None allowed for Class 1, 2 and 3.			3.6.2.1 Table 3-6
Cracks, External Foil	Allowed if cracks do not extend into plating.			3.6.2.1 Table 3-6
Cracks, Internal Foil	Allowed on only one side of hole provided cracks do not extend through foil thickness.	None allowed.		3.6.2.1 Table 3-6
Cracks, Laminate	Cracks in Zone B or originating in Zone A and into Zone B not greater than 150 µm [5,906 µin].	Cracks in Zone B or originating in Zone A and into Zone B not greater than 80 µm [3,150 µin].		3.6.2.4
	Cracks between two uncommon conductors in either horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.			
Crazing	Imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors.			3.3.2.2
Delamination/Blistering (Visual)	Acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns.			3.3.2.3
Delamination or Blistering	If present evaluate entire board per 3.3.2.3.	No evidence of delamination or blistering		3.6.2.5
Dewetting	Solder connection: 15%.	Solder connection: 5%.		3.5.4.5
	Conductors and planes are permitted.			
Dielectric Thickness	The minimum dielectric spacing **shall** be specified on the procurement documentation.			3.6.2.15
Dielectric Withstand Voltage	No requirement.	Spacing 80 µm [3,150 µin] or greater, 500 Vdc Time: 30 sec (+3, -0) Spacing less than 80 µm [3,150 µin], 250 Vdc Time: 30 sec (+3, -0)		3.8.1, Table 3-10
Dimensional Requirements	As specified in procurement documentation.			3.4
Edge Board Contact, Junction of Gold Plate to Solder Finish	Copper: 2.5 mm [0.0984 in]	Copper: 1.25 mm [0.04291 in]	Copper: 0.8 mm [0.031 in]	3.3.8
Edge Board Contact, Junction of Gold Plate to Solder Finish	Gold: 2.5 mm [0.0984 in]	Gold: 1.25 mm [0.04291 in]	Gold: 0.8 mm [0.031 in]	3.3.8
Edge Connector Lands	No cuts or scratches that expose nickel or copper; Pits, dents, or depressions accept if not exceed 0.15 mm [0.00591 in] in longest dimension with no more than three per land, and not appear in >30% of lands.			3.5.4.4
Edges (Visual)	Nicks or haloing do not penetrate more than 50% of distance from edge to nearest conductor or 2.5 mm [0.0984 in], whichever is less.			3.3.1
Electrical Requirements				3.8

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Etchback (When Specified)	Between 5 µm [197 µin] and 80 µm [3,150 µin] with a preferred depth of 13 µm [512 µin]. Shadowing is permitted on one side of each land.			3.6.2.6
Final Finish Coverage (Areas not to be Soldered)	Exposed copper on areas not to be soldered is permitted on 1% of the conductor surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor edges.			3.5.4.7
Foreign Inclusions	Translucent and other particles acceptable provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.			3.3.2.4
Fungus Resistance	No fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.			3.10.3
Haloing	Does not penetrate more than 2.5 mm [0.0984 in] or 50% of distance to closest conductor, whichever is less.			3.3.1
Hole Size and Hole Pattern Accuracy	As specified in procurement documentation. Applicable IPC-2220 design series requirements **shall** apply if not specified.			3.4.1
Impedance Testing	As specified in procurement documentation; TDR used for electrical testing, but for large impedance tolerances (± 10%), mechanical measurements from a microsection utilizing a special test coupon.			3.10.6
Inclusions, Innerlayer (Inclusions Between Interface of Internal Land and Through-Hole Plating)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	None allowed.	3.6.2.1 and Table 3-6
Insulation Resistance (As Received)	As received: Maintain electrical function.	As received: 500 megohms.		3.10.9 and Table 3-11
	After exposure to moisture: Maintain electrical function.	After exposure to moisture: 100 megohms.	After exposure to moisture: 500 megohms.	3.8.4 and Table 3-11
Isolation (Circuit Shorts)	Isolation resistance between conductors **shall** meet values established in the procurement documentation; 200 volt minimum for manual testing for at least five seconds; for automated tests, if min voltage not specified, use default value in Table 1-2.			3.8.2.2
Laminate Integrity	See voids, laminate.			3.6.2.3
Lifted Lands	Lifted lands are allowed on the thermally stressed microsection.			3.6.2.10
Lifted Lands (Visual)	No lifted lands on the delivered (nonstressed) printed circuit board.			3.3.4
Marking (Visual)	Conductive marking must be compatible with materials, and not reduce electrical spacing requirements.			3.3.5
Material				3.2
Measling	Measling **shall** be acceptable except for high-voltage applications.			3.3.2.1
Mechanical Shock	Board **shall** pass test requirements of 3.8.2 after mechanical shock.			3.10.5
Metal Cores, Horizontal Microsection	Wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material **shall not** reduce electrical spacing between adjacent conductive surfaces to <0.100 mm [0.00394 in]. Wicking and/or radial cracks **shall not** exceed 75 µm [2,953 µin] from the plated-through hole edge into the hole-fill.			3.10.10
Metal Core, Internal Spacing	Minimum between metal core, core wall, other conductors 100 µm [3,937 µin]			3.6.2.14
Minimum Layer/ Copper Foil Thickness	See Table 3-7.			3.6.2.12
Minimum Surface Conductor Thickness	See Table 3-8.			3.6.2.13
Moisture and Insulation Resistance	No measling, blistering or delamination in excess of that allowed in 3.3.2; insulation resistance meet requirements of Table 3-11; moisture and insulation resistance testing according to IPC-TM-650, Method 2.6.3.			3.8.4
Nailheading	Acceptable	Acceptable	Acceptable	3.6.2.17
Negative Etchback	Not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.	Not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.	Not to exceed 13 µm [512 µin] if etchback not specified on procurement documentation.	3.6.2.8 and Figure 3-9

Characteristic Inspection	Requirements Class 1	Class 2	Class 3	Requirement Paragraph
Nicks and Pinholes in Ground or Voltage Planes	Maximum size 1.5 mm [0.0591 in] with not more than six per side, per 625 cm^2	Maximum size 1.0 mm [0.0394 in] with not more than four per side, per 625 cm^2.		3.5.4.1
Nonwetting	For tin, tin/lead reflowed, or solder coated surfaces, not permitted on any conductive surface where a solder connection will be required.			3.5.4.6
Organic Contamination	Tested according to IPC-TM-650, Method 2.3.38 or 2.3.39, with no positive visual id of organic contamination.			3.10.2
Outgassing	Testing in accordance to procurement documentation; not resulting in a weight loss of more than 0.1%.			3.10.1
Pink Ring	Acceptable.			3.3.2.9
Plating Adhesion	No portion of protective plating or conductor pattern foil **shall** be removed. Testing in accordance with IPC-TM-650, Method 2.4.1.			3.3.7
Plating Folds, Inclusions	Must be enclosed and minimum copper plating thickness is met			3.6.2.1, Table 3-6
Plating Integrity, Plated-Through Holes	Properties specified in Table 3-6.			3.6.2.1
Plating Thickness, Copper, Blind Vias	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 25 µm [984 µin] Min. 20 µm [787 µin]	3.6.2.11, Table 3-2
Plating Thickness, Copper, Blind Microvias	Avg. 12 µm [472 µin] Min. 10 µm [394 µin]	Avg. 12 µm [472 µin] Min. 10 µm [394 µin]	Avg. 12 µm [472 µin] Min. 10 µm [394 µin]	3.6.2.11, Table 3-2
Plating Thickness, Copper, Buried Via Cores	Avg. 13 µm [512 µin] Min. 11 µm [433 µin]	Avg. 15 µm [592 µin] Min. 13 µm [512 µin]	Avg. 15 µm [592 µin] Min. 13 µm [512 µin]	3.6.2.11, Table 3-2
Plating Thickness, Copper, Buried Vias > 2 Layers	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 25 µm [984 µin] Min. 20 µm [787 µin]	3.6.2.11, Table 3-2
Plating Thickness, Copper, Surfaces and Holes	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 20 µm [787 µin] Min. 18 µm [709 µin]	Avg. 25 µm [984 µin] Min. 20 µm [787 µin]	3.6.2.11, Table 3-2
Plating, Coating Thickness	See Table 3-2.			3.6.2.11, Table 3-2
Plating and Coating Voids in the Hole (Visual)	Copper: three voids per hole in <10% of holes.	Copper: one void per hole in < 5% of holes.	Copper: none.	3.3.3
	Finished Coating: five voids per hole in <15% of holes.	Finished Coating: three voids per hole in <5% of holes.	Finished Coating: one void per hole in <5% of holes.	
	Areas of contamination or inclusions not to exceed 5% of each side of the interconnection or occur in the interface of the copper cladding on the core and the copper plating in the hole wall.			
Plating Voids	Meet requirements established in Table 3-6.	No more than one void per specimen, regardless of length or size. No plating void in excess of 5% of total flex PCB thickness. No plating voids evident at internal layer and PTH hole wall interface. No circumferential plating voids greater than 90°.		3.6.2.2
Repair	As agreed upon by user and supplier.			3.11
Resin Fill of Blind and Buried Vias	No fill requirement for blind vias. 60% fill for laminating resin for Class 2 and Class 3 buried vias.			3.6.2.16
Rework	Does not affect functional integrity of board.			3.12
Scratches, Dents, and Tool Marks	Does not bridge conductors, expose fibers > allowed in 3.3.2.4 and 3.3.2.5, and do not reduce dielectric spacing below minimum.			3.3.2.6
Separation Along Vertical Edge of External Land	Allowed provided the separation does not extend beyond the vertical edge of the external copper foil.			3.6.2.1, Table 3-6

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	**Class 2**	**Class 3**	
Separation, Innerlayer (Separation at the Interface Between Internal Lands and Through-Hole Plating	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	None allowed.	3.6.2.1, Table 3-6
Separation, Plating	Allowed at knee, maximum length 130 µm [5,118 µin]	None allowed.	None allowed.	3.6.2.1, Table 3-6
Shorts to Metal Substrate	Capable of withstanding 500 Vdc. No flashover or dielectric breakdown.			3.8.3
Smear Removal	Shall be sufficient to completely remove resin from surface of the conductor interface. **shall not** be etched back greater than 25 µm [984 µin]; random tears or drill gouges which produce small areas where the 25 µm [984 µin] depth is exceeded **shall not** be evaluated as smear removal.			3.6.2.7
Solder Resist (Solder Mask)				3.7
Solder Resist Coverage	Conductors not to be exposed or bridged by blisters in solder resist areas. For exposed dielectric, encroachment on lands, blistering, pits and voids in dielectric areas and board edge chipping, see 3.8.1.			3.7.1
Solder Resist Cure and Adhesion	No tackiness, delamination or blistering; maximum loss of adhesion after tape test per Table 3-9.			3.7.2
Solderability (Visual)	Solderability testing and accelerated aging will be in accordance to J-STD-003.			3.3.6
Special Requirements (When Specified)	As specified in procurement documentation.			3.10
Structural Integrity	Shall meet structural integrity requirements for thermally stressed (after solder float) evaluation coupons specified in 3.6.2.			3.6
Surface Microvoids	Not exceed 0.8 mm [0.0315 in] in longest dimension, bridge conductors, nor exceed 5 % of printed board area per side.			3.3.2.7
Solderable Surface Mount Lands (Rectangular)	Defects along edge of land not >30%; internal defects not >20%.	Defects along edge of land not >20%; internal defects not >10%.		3.5.4.2.1
	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. One electrical test probe mark allowed within the pristine area for Class 1, 2 and 3.			
Solderable Surface Mount Lands (Round)	Defects along edge of land not radially extend towards center by more than 30% of the diameter of the land and not extend more than 30% around the circumference of the land.	Defects along edge of land not radially extend towards center by more than 20% of the diameter of the land and not extend more than 20% of the circumference of the land.		3.5.4.2.2
	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. One electrical test probe mark allowed within the pristine area for Class 1, 2 and 3.			
Thermal Shock	Testing/evaluation according to IPC-TM-650, Method 2.6.7.2, with temp range between -65 °C to 125 °C [-85 °F to 257 °F]. An increase in resistance of 10% or more **shall** be considered a reject and **shall** meet requirements of Table 3-6 after cycling.			3.10.8
Thermal Stress Testing	Specimens conditioned by baking at 120 °C to 150 °C [248 °F to 302 °F] for six hours, depending on thickness and according to IPC-TM-650, Method 2.6.8. After microsectioning, plated-through holes **shall** be examined for foil and plating at 100X ± 5%. Referee examinations made at 200X (± 5%).			3.6.1
Vibration	Board **shall** pass test requirements of 3.9.2 after vibration cycling.			3.10.4
Visual	Finished product **shall** be examined, be of uniform quality, and conform to 3.3.1 through 3.3.9.			3.3
Voids, Laminate	Voids in Zone B not >150 µm [5,906 µin].	Voids in Zone B not >80 µm [3,150 µin].	Voids in Zone B not >80 µm [3,150 µin].	3.6.2.3
Voids in Surface	Acceptable if not >0.8 mm [0.031 in] in longest dimension or exceed 5% of the board area per side.			3.3.2.7
Weave Exposure	Acceptable if does not reduce conductor spacing below minimum.			3.3.2.5

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Wicking	125 µm [4,921 µin] maximum	100 µm [3,937 µin] maximum	80 µm [3,150 µin] maximum	3.6.2.1, Table 3-6
Wire Bond Pads	Final conductor finish as specified in 1.3.4.2 for GWB-1, GWB-2 or ENIG. Final finish coating per Table 3-2 for applicable coating. Pristine area **shall** have maximum surface roughness of 0.8 µm [32 µin] RMS as measured in accordance with Method 2.4.15. No pits, nodules, scratches, electrical test probe marks within the pristine area that violates RMS requirement.			3.5.4.3
Workmanship	Shall be free of defects and of uniform quality - no visual of dirt, foreign matter, oil, fingerprints.			3.3.9

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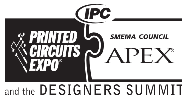

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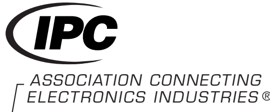

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IPC-6012B with Amendment 1

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The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

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