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CIA

GENERAL SPECIFICATION

For Double-sided and Multi-layer Printed Circuit Boards

Version 1.4

Records of Revision

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1.0 GENERAL INFORMATION

1.1 SCOPE

1.1.1 This specification is established for double-sides and multi-layer Printed Circuit Boards (PCB), which covers the detail requirements of the manufacturing and quality control / assurance for PCB supplier.

1.1.2 This specification is a common document, also is the backup document of Product Specification of Double-sided and Multilayer PCB, which shall applies to all double-sided and multilayer PCBs purchased by CIA.

1.1.3 PCB supplier shall be required to comply with all requirements of this specification. CIA must approve any deviation against this specification in written reply.

1.1.4 This specification is also the acceptable standard of Incoming Inspection of CIA. The batch shall be rejected if the PCB is not in accordance with this specification.

1.2 PURCHASE DOCUMENTS AND PRIORITY OF DOCUMENTATIONS

1.2.1 Purchase Documents

CIA shall provides following Purchase Documents to supplie as manufacturing information for each item:

a. Purchase order
b. Gerber files (Layout of Pattern, Soldermask and Silkscreen, Drilling file etc.)
c. Mechanical drawing,
d. Product Specification,
e. Other documents if need to be applied.

1.2.2 Priority of documents

The requirements specified in this specification should be considered as “general”. In case of discrepancy between this specification and other purchase documents provided or specified by CIA, the sequence of priority for different requirements must be kept as following:

First: Purchase Order, Gerber file and Mechanical drawing
Second: Product Specifications
Third: This Specification (CIA General specification)
Last: Related PCB industry standards as paragraph 2.0 listed.

1.3 VERIFICATION BEFORE PRODUCTION

The PCB supplier is responsible for:

--Checking discrepancies between the requirements in the Gerber file, Drilling file, Mechanical drawing, Product Specification and other Purchase Documents provided by CIA. Any discrepancies must be submitted to CIA and the production of PCBs should be started only after receiving a written reply or indication from CIA.

--Ensuring that the production tools and the materials are in accordance with CIA requirements, or may be purchased in time without difficulty. The requirements must be fulfilled before accepting the purchase order or establishing the price or delivery time.

--Ensuring that his process includes all quality assurance provisions and apparatus needed for all tests included in process control and final audit, and for the intermediary tests, must perform according to the Purchase Documents and related IPC standards.

2.0 APPLICABLE SPECIFICATIONS

In case of not specified in Purchase Documents, the latest version of following specifications must be met for the layout design and manufacturing of PCB:

IPC-6011	Generic Performance Speicification for Printed Boards
IPC-6012	Performance Specification for Rigid Printed Boards
ANSI/IPC-A-600	Acceptabitity of Printed Boards
IPC-6016	Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards
IPC-2615	Printed Board Dimensions and Tolerances
IPC-4101	Laminate / Prepreg Specification for Printed Boards
IEC-249	Base materials for printed circuits
IPC-4104	Specification for High Density Interconnect (HDI) and Microvia Material
IPC-4562	Metal Foil for Printed Wiring Applications
UL-94	Standard for Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
UL-796	Standard for Safety – Printed Wiring Board
IPC-2222	Design Rigid Board
IPC-TM-650	Test Method of Printed Boards
IPC-SM-840	Qualification and Performance of Permanent Solder Mask – Includes Amend 1
IPC-7721	Repair and Modification of Printed Circuit Board and Electronic Assemblies
ANSI/J-STD-003	Solderability Tests for Printed Boards

Notes: Generally, IPC Class 2 is applied to all cases and Class 3 only for high performence products with specially noted.

3.0 MANUFACTURING REQUIREMENTS

3.1 MATERIALS

3.1.1 Qualified Raw Materials

The raw material supplier and product type as following table showed are qualified by CIA. They must be used on all CIA duoble-sided (D/S) and multilayer (M/L) PCBs unless otherwise specified on Purchase Documents.

Materials	Product Characteristices	Application D/S or M/L	First Supplier		Second Supplier	
			Supplier Name	Product Type	Supplier Name	Product Type
Copper Clad Laminate (CCL)	FR-4 Tg ≥ 130℃	D/S & M/L	SHENGYI	S1141 S1600	King Board ITEQ	KB6160/C IT588
	FR-4 Tg ≥150℃	D/S & M/L	SHENGYI	S1000	ITEQ	IT158
	FR-4 Tg ≥170℃	D/S & M/L	SHENGYI	S1170 S1000-2	ITEQ	IT180
	CEM3	D/S	SHENGYI	S2130 S2600	NANYA	CEM 3-10
Solder Mask	LPI	D/S & M/L	TAIYO	PSR2000 PSR4000	TAMURA	DSR2200
Peelable Solder Mask	Heat Cure	D/S & M/L	PETERS	SD 2955	PETERS	SD 2954 SD 2950
UL File Number	UL File Number of SHENGYI of CCL supplier is E109769.					
	UL File Number of NAN YA of CCL supplier is E98983 (S)					
	UL File Number of King Board of CCL supplier is E123995					

Notes : *1.Other similar type material not specified in this form can be used only after get written approval from* CIA.
2. When the raw materials have to be defined before production, its data sheet, including Material Safety Data Sheet (MSDS), must be provided to CIA. *At same time the EACEM list for environmentally relevant substances must be declared and provided to* CIA *too.*

3.1.2 CCL Requirements

Unless otherwise specified on the Purchase Documents, the CCL used for manufacturing of Double-sides and Multi-layer PCB must be glass-fiber base, epoxy resin and conforming to IPC-4101, NEMA LI-1 or IEC249 standard with UL 94-V0 flammability class.
The base material is to be evenly colored. Color variations in a panel or a piece are un-acceptable.

3.1.3 Prepreg and Core Requirements

a. Unless otherwise specified on the Purchase Documents, the base material for inner-layers (Core) and the B-stage material (Prepreg) for dielectric shall be glass-fiber base, epoxy resin with UL 94V-0 or better flame rating; The thickness, appeance and performace must conform to the requirements of the latest version IPC-4101 Class 2.

b. The Prepreg should be tested with each production run for its ability to form adhesion throughout the multilayer composite. The quality of the Prepreg must be tested for resin quality and consistency with the supplier's lamination process. The test of cure shall be as agreed between supplier and user, but shall include "resin flow", gel time, resin and volatile content and viscosity as described in IPC-4101 latest version.

c. Dielectric Constant of Core and Prepreg must be within 4.2 and 4.5 when the CCL is applied to the controlled impedance PCBs.

3.1.4 Copper Foil

Copper foil thickness of each item shall be specified in the Purchase documents and conform to the requirements of IPC-4101 latest version. The tolerance and other quality requirements shall conform to IPC-4562 latest vesion.

3.1.5 Soldermask

All performance of soldermask shall conform to the requirements of IPC-SM-840 class T latest version.

3.2 CAM AND TOOLS PREPARATION

3..2.1 Manufacturing Information

The Manufacturing Information shall be provided by CIA as Paragraph 1.2.1 introduced.

3.2.2 Gerber File Checking

a. Supplier may increase line widths and pads for compensating undercut only. The supplier must not move any feature without written approval from CIA

b. The nominal finished feature size after etching must be equal to the Gerber file feature size within the tolerance specified in Purchase Documents and this specification. Contact CIA for written approval if the nominal artwork dimensions cannot be met, especially for controlled impedance PCB's.

c. All other data modifications (i.e. soldermask clearances, thermal reliefs, removal of non-functional pads, etc) also require written approval from CIA.

3.2.3 Net-List Checking

a. The supplier must perform a gerber to net-list comparison if a net list file is provided with the design data. Contact CIA if any discrepancies are found.

b. The supplier must also compare an extracted net list before and after any gerber modifications to ensure that these modifications did not result in a functional change.

3.2.4 Impedance Verification

Suppliers must calculate the Impedance value based on the layer lay-up, width and thickness of transmission line, dielectric constant of CCL and so on to verify the impedance of design. Any deviation must be submitted to CIA for written approval.

3.3 CCL AND PREPREG CUTTING

3.3.1 General

Unless otherwise specified, the qualified suppliers and types of CCL, prepreg and RCC as Paragraph 3.1.1 listed must be used in any case.

3.3.2 Requirements

a. The working panel size of CCL and prepreg may be free to choose by PCB supplier in order to get the best efficiency, but CCL, prepreg and RCC must be sure to use same supplier and same type in same PCB item, their X and Y direction must also be same in same working panel.

b. CCL must be baked at least 4 Hours with over Tg temperature in order to get the better dimension stability.

3.4 INNER LAYER TREATMENT

3.4.1 Process of Treatment

If not specified on the Purchase Documents, the inner layer of all CIA multi-layers must be chemically treathed with a lamination adhesion promoter, the preference is **Black Oxide**, Brown Oxide treathment or other treatment type must be officially approved by CIA before use.

3.4.2 Copper Foil Thickness of Inner Layer (without plating)

The copper foil thickness of inner layer must be met following minimum requirements after treatment:

CCL Foil Thickness	Starting Copper Foil Thickness	Min. Copper Thickness After Treatment	Figure
3/8 oz	12μm	8μm	Min. Cu Thickness
1/2 oz	17μm	12.0μm	
1 oz	35μm	25.0μm	
2 oz	70μm	56.0μm	
3 oz	105μm	91.0μm	
4 oz	140μm	122.0μm	

Notes: The requirements of inner layer Cu thickness with plated are specified in Paragraph 3.8.2.

3.4.3 Automated Optical Inspection (AOI)

All signal inner layers must be 100% inspected by AOI.

3.4.4 Other Requirements

The inner layer shall be consistent color and shade, and be free of physical damage or inclusions of debris. There shall be no evidence of chemical attack of the oxide treatment (pink ring) when the product is inspected at 10X magnification.

3.5 MULTILAYER LAMINATE

3.5.1 Lay-up Construction

The lay-up construction of multiplayer shall be defined in Purchase Documents for each PCB item.

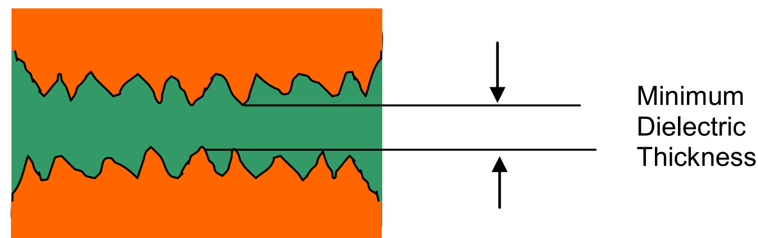
3.5.2 Tolerance of dielectric material thickness

No	Nominal Dielectric Thickness	Allowed Tolerance
1	T ⩽ 0.125 mm	± 0.025 mm
2	0.125 ＜T ⩽ 0.175 mm	± 0.038 mm
3	0.175 ＜T ⩽ 0.300 mm	± 0.050 mm
4	0.300 ＜T ⩽ 0.510 mm	± 0.064 mm
5	0.510 ＜T ⩽ 0.760 mm	± 0.076 mm

3.5.3 Requirements

a. The multilayer after laminate must be able to run over user's re-flowing machine or wave solder machine per J-STD-003 for 2 times without prior baking, there must be no any delaminations and blister, or evidence of measling on board.

b. The multilayer after laminating, following requirements must be met observing by cross-section:
--Registration inner layer to inner layer must be within +/- 0.100 mm of nominal size.
--Minimumm annular ring-internal layers must not be ＜ than 0.025mm or no breakout.
--The distance of inner layer metal ring or plane to plated or not plated hole wall shall not be less than 0.12mm if the Purchase Documents does not specify a value.
--If there is no specified dielectric thickness in Purchase Documents, the minimum thickness must not be less than 0.09mm. Measured as following figure showed:



Notes: For Impedance controlling PCB, CIA *would specify the special dielectric thickness requirement and measuring method.*

c. After thermal stress test, the multilayer must be no following defects observing by cross-section:
--End of copper land must not be lifted from the base material.
--Laminate Void must not be less than 0.08mm and violated minimum dielectric spacing.

d. After laminating, the defects of crazing, measling, blistering and delamination must be conforming to the requirements of IPC-A-600 Class 2 latest version.

3.6 DRILLING

3.6.1 Drilling Process

The Hole is drilled by mechanical machine or laser machine is depended on different type of PCBs (HDI or common multi-layer). The drilling method shall be specified on Purchase Documents for each PCB item.

3.6.2 Hole Diameter Tolerance (After drilling without plating)

No	Nominal Size (mm)	Tolerance (mm)
1	0.3≤d≤2.0	-0.00/ + 0.10
2	2.0≤d≤5.0	-0.05/ + 0.10
3	5.0≤d	-0.1/ + 0.2
4	Reference holes	-0.05/ + 0.05

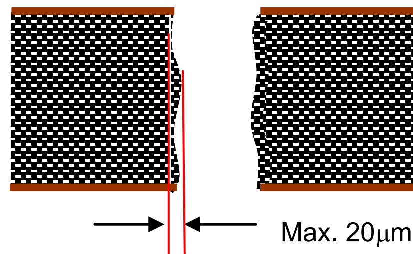
For press-fit hole please refer to paragraph of 3.17

3.6.3 Requirements

a. When dimension of hole center to hole center ≤ 300mm, which registration should be less than or equal to 0.075mm .

b. When dimension of hole center to hole center ＞300mm, which registration should be less than or equal to 0.100mm

c. Maximum roughness should not be more than 20μm as following figure showed:



For press-fit hole please refer to paragraph of 3.17

d. The quality of hole walls after plating must be conforming to following requirements:
--Wicking must not exceed 0.10mm observing by cross-section.
--Wicking reduced conductor spacing must not be less than specified minimum value on Purchase Documents observing by cross-section.

3.7 PLATED THROUGH HOLE (PTH) –Electroless Copper Plating

3.7.1 PTH Process

The process with chemical immersion Cu is required and other process such as Shadow Process is not allowed without written approval from CIA.

3.7.2 Requirements

a. The de-smear must be controlled under following requirements:

-After thermal stress test, PCB hole wall (laminate to plated copper) must be no any separation observing by cross-section.
--Etch-back must not be less than 5µm or greater than 80µm observed by cross-section.
--Negative etch-back must not exceeds 25µm observed by cross-section.

b. After PCB finished, the Plating Voids must not be more than 1 void per Cross-section coupon, the acceptable size of void refer to IPC-A-600 class 2.

3.8 COPPER PLATING

3.8.1 Copper Plating Thickness in Hole

Following Cu plating thickness in hole must be met for different process applications unless otherwise specified:

a. Mechanical Drilling

Process Applications	Hole diameter ＞0.3mm			Hole diameter ⩽0.3mm		
	Min. avg.	Min. thin area	Deviation	Min. avg.	Min. thin area	Deviation
Through Holes	25µm	20µm	20-50µm	20µm	15µm	15-40µm
Blind Via	20µm	18µm	18-50µm	18µm	15µm	18-40µm
Buried Via	15µm	13µm	13-40µm	15µm	13µm	13-40µm

b. Laser Drilling

Process Applications	Hole diameter ＞0.15mm			Hole diameter ⩽0.15mm		
	Min. avg.	Min. thin area	Deviation	Min. avg.	Min. thin area	Deviation
Blind Via	12 µm	10 µm	10-30µm	12 µm	10 µm	10-30µm

3.8.2 Copper Plating Thickness on Conductor

The copper plating thickness on conductor after PCB finishing is depended on different basic foil thickness of CCL, following conditions must be met unless otherwise specified:

Nominal Foil Thickness of CCL	Required Thickness	
	Plated Thickness	Min. Finished Thickness
1/2 oz	25-50µm	38µm
1 oz	18-35µm	46µm
2 oz	15-30µm	79µm

Notes: This requirement also applies to inner layer copper thickness with plated.

3.8.3 Tolerance of Diameter of Plated Though Holes

If not specified in Purchase Documents, the tolerance of finished plated hole diameter must fulfill following requirements:

No	Nominal Hole Size	Tolerance
1	0.3⩽d⩽2.0mm	±0.075 mm
2	d＞2.0mm	±0.1mm

3	Via in PAD (VIP) Finished	0.25mm max (Via in PAD (VIP) after Drilling should be 0.3mm max)

For press-fit hole please refer to paragraph of 3.17

3.8.4 Plating Adhesion

The adhesion between the hole copper plating and the inner layer or base copper of laminate shall withstand all tests, including thermal shock, thermal stress, and rework, when tested in accordance with IPC-6012 or IPC-6013.

3.8.5 Plating Voids, Nodules and Roughness

a. The plating void must not be more than 1 void of plating per cross-section or production board, regardless of length or size.

b. The Plating Nodule or Roughness must not reduce the plating thickness or hole diameter below minimum requirement. There should be no evidence of nodules on the surface of component or test lands/pads when viewed at 3X magnification.

3.9 PATTERN (CONDUCTOR)

3.9.1 Tolerance of Conductor Width and Spacing (unit: mm)

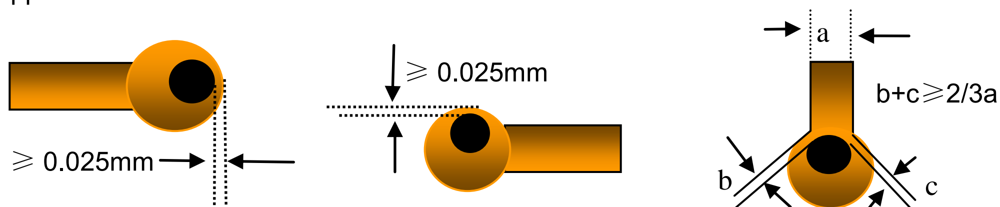
Conductor Type	Nominal Conductor Width	Tolerance	
Line without Controlled Impedance	⩽0.25mm	Width / Spacing	Nominal +/-20%
	> 0.25mm	Width / Spacing	Nominal +/-0.05
Line with Controlled Impedance	⩽0.25mm	Width / Spacing	Nominal +/-0.025
	> 0.25mm	Width / Spacing	Nominal +0.03/-0.03
SMT Pads	Nominal	Width < 20mils	-0.05 /+0.0
		Width >20 mils	+/-10%
Gold Fingers	Nominal	Width	-0.05 /+0.0

3.9.2 Registration

a. Registration of pattern to pattern on same side must be equal or less than 0.075mm.

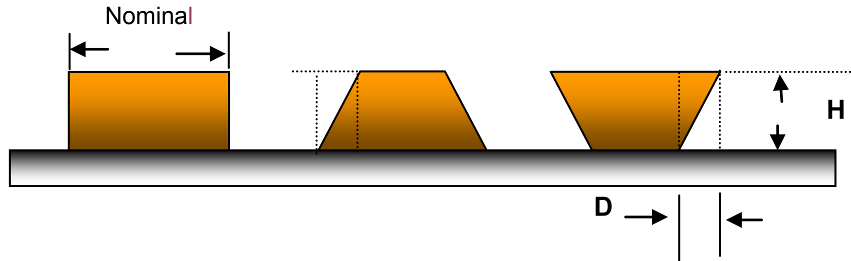
b. Registration of topside pattern to bottom side pattern must be equal or less than 0.100mm.

c. Registration of PAD to Hole must meet following conditions regardless with supported hole or unsupported hole.



3.9.3 Undercut

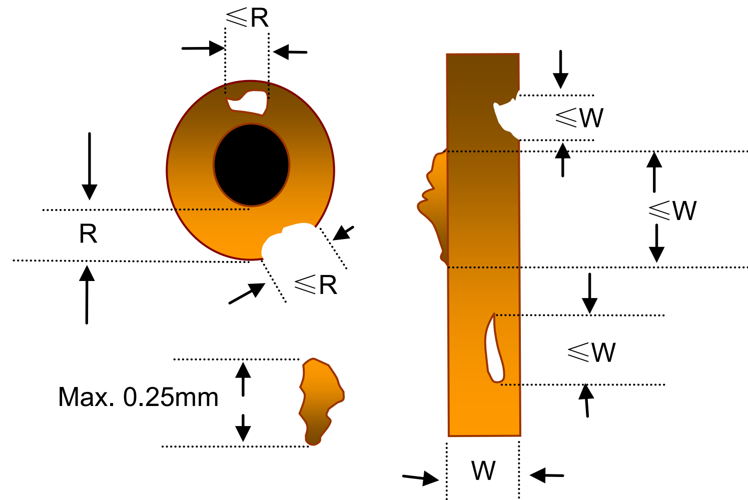
Following must be met unless otherwise specified:



Conductor with 1/2 oz base copper foil: H / D ⩾ 1.7
Conductor with 1 oz base copper foil: H / D ⩾ 1.2
Conductor with 2 oz base copper foil: H / D ⩾ 0.8

3.9.4 Other Requirements

a. The width of any copper residues, isolated edge roughness, nicks, pinholes, and scratches exposing base material must not reduce the conductor width or spacing less than the tolerance specified in Paragraph 3.9.1, which maximum length must meets following conditions too:



b. For PCBs with controlled impedance requirement, the conductor and its edge must be sharp and without nicks, protrusion, pinhole, dent and scratches; in space of conductors, there should be no any copper residues.

c. There shall be no occurrence (edge roughness, nicks, etc.) is greater than 10% of the conductor length or 10mm, whichever is less.

3.10 SOLDERMASK (Solder Resist)

3.10.1 Soldermask Type
Unless otherwise specified on the Purchase Documents, only qualified soldermask suppliers and type listed on Paragraph 3.1.1 may be used. For use of other types of soldermask, a special approvel from CIA must be obtained.

3.10.2 Soldermask Color

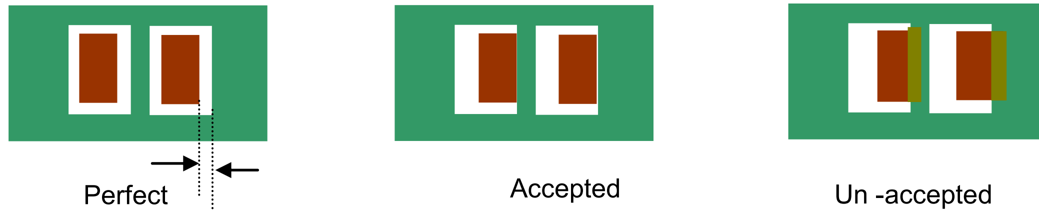
Soldermask Color shall be as specified in Purchase Documents, if not otherwise specified color should be green and finish shall be semi-gloss or matte.

3.10.3 Soldermask Thickness

On the midpoint of conductor, the soldermask thickness must be more than 10µm; on the corner of conductor, the soldermask thickness must be more than 6µm. But for the maximum thickness must not be higher than the SMT pads of PCBs,

3.10.4 Soldermask Registration

There shall be no encroachment of soldermask onto component or test lands/pads unless intentionally designed to do so. Maximum clearance shall be from 0mm to 0,1mm (max distance between PADs edge and Solder edge)



3.10.5 Soldermask Plugging for Via Holes

a. If via plugging with soldermask is required, a minimum of 80% of the vias must be completely sealed with soldermask.

b. For any BGA, CGA or CSP sites where via plugging is required, 100% of the vias must be completely sealed with soldermask. The thickness of any soldermask plug above the finished copper must not exceed 50um.

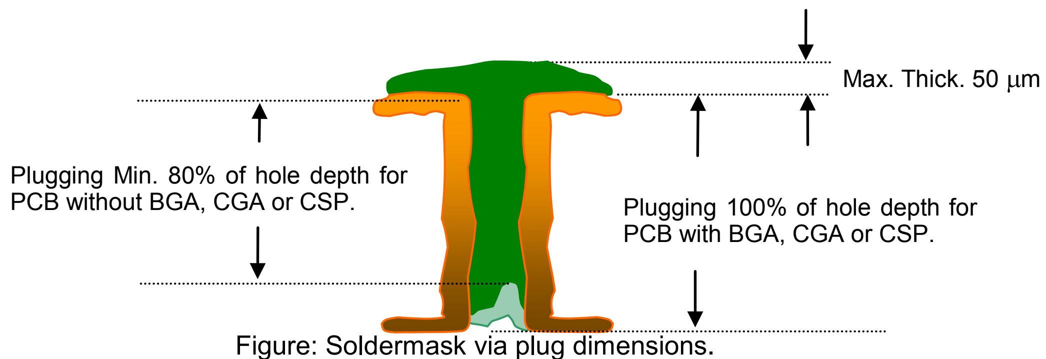


Figure: Soldermask via plug dimensions.

3.10.6 Soldermask Covering for Via Holes

If via covering with soldermask is required, PCB supplier must be sure that no tin/lead or flux will flow out from the vias during assembly.

3.10.7 Other Requirements

a. The soldermask must be capable of withstanding immersion in a molten solder bath at a temperature of 288℃ minimum for minimum 10 seconds with no blister and delamination.

b. There shall be no discoloration, blistering, cracking, peeling or flaking of the solder mask, and the mask shall also be no the internal voids and other inclusions or discoloration spots. The other performance of solder mask of finished PCBs shall fully meet the requirements of IPC-SM-840 Class T.

3.11 PEELABLE SOLDERMASK

3.11.1 Type of Peelable

The peelable solder mask type must be PETERS SD 2955 or PETERS 2954 or PETERS 2950 as Paragraph 3.1 specified.

3.11.2 Requirements

If peelabel solder mask is required in Purchase Documents, which must be applied as follows:

a. Thickness must be 0.5mm + 0.2/- 0.2 mm .

b. Peelable solder mask must completely encapsulate the required area of coverage. When applied over holes shall not protrude on the other sider of the PCBs.

c. Peelable solder mask must be chemically compatible with all assembly processes.

d. Peelable solder mask must be applied to withstand multiple (⩾ 3 times) soldering process cycles.

e. Peelable solder mask must be easily removable with no residue left on the board surface or holes.

3.12 MARKINGS

3.12.1Required markings

Unless otherwise specified, each individual board must have following markings for traceability by Copper or Silk-screen Legend, and which markings must not be located under a component site.

--Date code (week--/year--);
--UL flammability rating, Manufacturer Mark and UL File Number
--Electrical test mark.(TE or ET)
--For controlled impedance board is necessary to print a progressive number for each board of each Lot. In case of test Coupon must be printed separately from the board but showing same progressive No. as for the board.

Notes: All required markings should be sharply defined and fully legible. All marks shall be resistant to all normal cleaning solvents. The acceptability of marks must be accordance with the IPC-A-600 Class 2 latest version.

3.12.2 Silkscreen

Silkscreen should be in accordance with the silkscreen Gerber file and use permanent solvent-resistant ink. Color shall be white if not other specified in Purchase Documents. Registration shall be Max. 0.25 mm, and any markings on the pads must be removed.

3.12.3 Date Code

If not other requirement in Purchase Documents, the date code shall be screen-printed in positive legend on the PCBs, and with sequence of week/year.

3.12.4 UL Identification

The supplier's UL signature, as defined in the UL Recognized Component Directory, shall be present on each PCBs and remain visible after assembly of board is completed.

3.13 SURFACE FINISHS AND GOLD FINGER

3.13.1 General

a. The surface finish shall be specified in the Purchase Documents.

b. All product is to be Soldermask Over Bare Copper (SMOBC). Soldermask over Ni/Au or other application must be obtained written approval from CIA.

3.13.2 Hot Air Solder Leveling (HASL)

a. Solder Thickness Requirements:

--SMT pads with fine Pitch less than 0.076mm and BGA Devices:
Minimum thickness 1.0μm at geometric center
Maximum thickness 25μm at crest
Maximum thickness variation across a device site shall not be more than 18μm.

--All other pad sites:
Minimum thickness 1μm at geometric center
Maximum thickness 30μm

b. PCBs shall not be subjected to more than two times HASL.

c. Solder coating shall be uniform in appearance, with even texture, free of contamination, blisters, and slivers. There should be no exposed base metal or pure inter-metallic on any land or pad.

d. If PCBs have soldermask via plugs, vias must not be plugged with tin/lead. If boards have soldermask via covers, CIA still prefers vias not to be plugged with tin/lead. However, if vias with soldermask cover get plugged with tin/lead, PCB supplier must be sure that no tin/lead or flux will flow out from the vias during assembly course.

3.13.3 Electroless Nickel and Immersion Gold (ENIG)

a. Thickness: Min 0.075μm of immersion gold over 3 – 8 μm of electroless nickel.

b: It must pass 3 times Adhesion Test and no peel-off is allowed.

3.13.4 Electrolytic Gold over Electrolytic Nickel (used as etch-resist for solderable surfaces)

a. Thickness: 0.05 – 0.25 μm of electroplated hard gold over 3 – 10 μm of electroplated nickel.

b: It must pass 3 times Adhesion Test and no peel-off is allowed.

3.13.5 Electrolytic Gold over Electrolytic Nickel (Gold fingers or contact pads)

a. Thickness: Min 1.3 μm of plated hard gold over Min 5 μm of plated nickel. For Telecomunication PCB, special thickness of Ni/Au must be applied as Purchase Documents specify.

b. Au Hardness shall be more than 140 Knoop. Ni hardness higher than 150 Knoop

c. Purity of gold shall be more than 99.8%. Purity of nickel shall be more than 99.5%.

d: It must pass 3 times Adhesion Test and no peel-off is allowed.

e. There shall be no scratches or voids in plating. The edges of the contact pad or gold finger must be fully covered except where be beveled. The transition line between the gold plating and the conductor should be without any exposed copper.

3.13.6 Immersion Tin

a. Thickness must be Min 0.75μm. and less than 1.2um

b: It shall pass 3 times Adhesion Test and no peel-off is allowed.

3.13.7 Immersion Silver

a. Thickness must be Min 0.075μm.

b: It shall pass 3 times Adhesion Test and no peel-off is allowed.

3.13.8 Organic Solder-ability Preservative (OSP)

a. Approved OSP's are limited to Enthone OMI's Entek Cu-56 or 106A. Other similar type can be used only after get written approval from CIA.

b. The thickness must be controlled within 0.3μm to 0.5μm measured in chemical analysis method.

c. The PCBs with OSP finish must be capable of passing at least two times reflow soldering.

3.13.9 Solderability

a. Solderable surfaces must be compatible with multi-pass no-clean solder assembly processes. Lot based solderability testing must be performed in a manner that ensures this requirement.

b. Solder bath test must be used no-clean flux. Sample should be pre-baked at 150°C for 1 hour to simulate first pass assembly heat cycle.

--Solderability Test Condition: Temperature: 235℃ + 5 ℃/ - 0 ℃. Time: 3~5 second.

--Requirement: The PCBs surface which faced the solder bath has to be covered with a continuous, evenly distribute coating of solder, There may be minor faults such as pinholes up to 5% of the solder surface is acceptable.

c. The solderability of PCBs with any surface finish must be met above requirements within storing 6 months.

3.14 OUTLINE FABRICATION

3.14.1 Routing and Punching

a. The outline fabrication of PCBs shall be specified on Purchase Documents. Routing is required in any case. Punching must be approved in written by CIA in advance.

b. Following tolerance should be applied to any outline dimension if not other specify:

No	Nominal Dimension	Tolerance
1	0~200mm	+/- 0.10mm
2	201~400mm	+ /- 0.15mm
3	Slots	+/- 0.10mm
4	Slot Radius	1.20 Max.

c. Hole to edge of board registration shall be less than 0.15mm.

3.14.2 V-Scoring

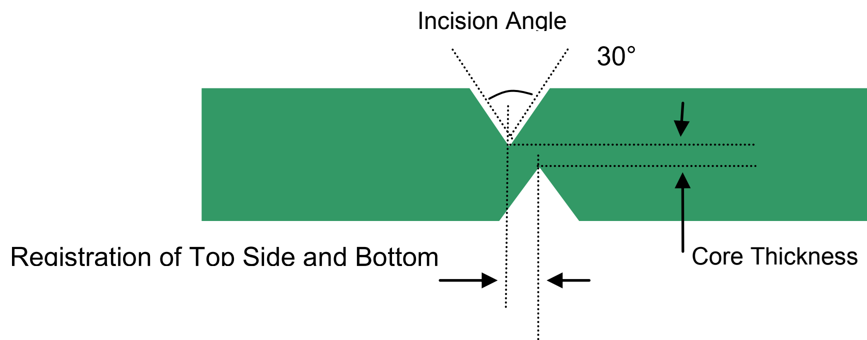
a. If the V-CUT is required, the incision angle of scoring should be 30 degree unless otherwise specified.

b. After scoring following core thickness should be required if not specified in Purchase Documents:

No	Nominal Board Thickness	Core Thickness after scoring	
		CEM-3	FR-4
1	0.8/1.0/1.2mm	0.5+/-0.1	0.3-0.4 +/-0.1
2	1.6/2.0mm	0.6+/-0.1	0.40 +/-0.1

c. Scoring Location: +/-0.10mm.

d. Registration of Top Side and Bottom Side: 0.10mm.



3.14.3 Beveling of Connector Edge

The beveling angle for gold finger should be 30 degree if not specified in Purchase Documents. The beveling "A" per edge shall meet following requirements:

0.4⩽ A ⩽0.6mm, when T⩾1.6mm

3.15 THICHKNESS AND TOLERANCE OF FINISHED BOARD

The thickness of finished board will be specified on Purchase Documents. If the tolerance does not be specified, +/- 10% of nominal must be met:

3.16 BOW AND TWIST OF FINISHED BOARD

Maximum allowable bow and twist must not exceed the following in any direction across the board:

a. 1.0% for boards using through hole components only. When the boards after thermal stress , which maximum bow and twist must be less than 1.3%.

b. 0.7% for boards using any surface mount technology. When the boards after thermal stress , which maximum bow and twist must be less than 0.9%.

c. 0.5% for boards using any Ball Grid Array (BGA), Column Grid Array (CGA), Chip Scale Packaging (CSP), or Flip-chip technology, with 0.3% in/in across any of these component areas themselves. When the boards after thermas stress , which maximum bow and twist must be less than 0.7%.

Notes: The measurement method please refer to IPC-TM-650 2.4.22

3.17 SPECIAL REQUIREMENTS FOR PRESS-FIT HOLE.

3.17.1 Dimension Characteristics Requirements

Pitch of Hole to Hole	Hole with Pitch 2.54mm	Hole with Pitch 2.50mm	Hole with Pitch 2.00mm
Finished Hole Size	1.0mm	1.0mm	0.6mm
Hole Diameter after drilling (mm)	1.15	1.15	0.7
Hole Tolerance after drilling (mm)	±0.03	+0.0/-0.03	±0.025
Hole Diameter after plating (mm)	0.98-1.08	+0.09/-0.06	0.55-0.65

Registration of hole to reference	Nominal Size ＜300 mm: +/-0.070 mm Nominal Size ⩾300 mm: +/-0.070 mm	Hole Center registration refer to first hole along X Y +/-0.070 mm Hole Center registration refer to first hole same block along X Y +/-0.050 mm
Hole Roughness	⩽20µm	

3.17.2. Physical Characteristics Requirements

No.	Physical Characteristics	Requirements	
1	Cu Plating Thickness	Minimum 20 µm Max 50 um	
2	Cu Hardness	Maximum 150 Knoop	
3	Finishing Thickness	Hot Air Solder Levering	1 µm to 30 µm
		Immersion Tin	0.75 µm to 1.2µm
		Immersion Silver	0.075 µm to 0.15µm
4	Insertion Strength	Maximum 185 N / contact	
5	Extraction Strength	Minimum 45 N / contact	
6	Insertion Times Per hole	Minimum 2 times	

3.18 PACKAGING

(1) 20 panels for each vacuum package
(2) Each vacuum packaging request desiccators (silica gel).
(3) Please print the CIA label stick on the box, and red tape on the carton which contains reports, see below:

(4) Each box weight cannot excess 20 Kg.
(5) For each shipment, a test report, cross-section and COC is request，need report for each date code.
(6) No need to separate the board by paper.
(7) The carton box must be in 3-ply.

4.0 QUALITY CONTROL AND ASSURANCE REQUIREMENT

4.1 AUTOMATED OPTICAL INSPECTION (AOI)

For innerlayer, all signal layer must be inspected by AOI. For PCB with contolled impedance requirement, the outlayer also must be inspected by AOI. If there are fine line in outlayer, PCB supplier is suggested to do AOI inspection too.

4.2 ELECTRIC TEST

4.2.1 Open/short Test

a. Unless otherwise specified, all boards must be 100% electrically tested for open/short using double access net-list testing. Test parameters shall be +250 volts with a maximum resistance threshold of 20 Ohms and 5 Meg Ohm isolation.

b. Each individual board that has passed electrical test must be marked with a permanent marking. (TE or ET)This marking must be in the same location on each board(on Component side), and must not encroach onto any metallic surface, tooling holes, or fiducial clearances. The mark must be legible after 6 assembly heat cycles and assembly cleaning processes. The mark must not be located under a component site.

4.2.2 Controlled Impedance

If controlled impedance is specified in the Purchase Documents, the supplier must provide a sample of the impedance coupons and TDR test results with the first shipment of the part number. The supplier must keep all coupons and reports at least 1 year.

4.3 MECHANICAL MEASUREMENT

The drilling and routing process must be checked frequently to ensure that the process keeps within the required mechanical tolerances.

4.4 CLEANLINESS

The cleanliness requirements described here pertain to before and after solder mask application. Cleanliness testing shall be performed in accordance with IPC6012 latest version. The acceptance criteria for bare PCBs shall be one quarter of the acceptance criteria of IPC6012 latest version. That is 0.78 micrograms of NaCl equivalent per square centimeter when using Ionogragh, 0.55 micrograms of NaCl equivalent per square centimeter for using Omega Meter TM. This testing shall be conducted on production boards on a statistically selected spot check basis.

4.5 STATISTICAL PROCESS CONTROL

Statistical process control (SPC) must be used for critical process control. The following elements are minimum requirements for this control system:

4.5.1 Control charts must be used on all critical process controlling. These charts must either be posted at each process or operation, or be readily available on nearby terminals or binders.

4.5.2 Specification limits must be defined and drawn on all control charts. These limits must either be based on the process supplier's recommendations or documented design of experiments.

4.5.3 Control limits must be defined within the specification limits and be drawn on all control charts. These limits are to be determined statistically or be tighter than the statistically defined limits.

4.5.4 Data points are to be plotted at regular intervals on all charts.

4.5.5 All operators must be trained to analyze trends in data points.

4.5.6 If a data point falls outside of a control limit, corrective action must be taken immediately and the process must be verified to be back in control.

4.5.7 Collection of data is to be often enough that material build during out of specification intervals can be quarantined by the PCB supplier. This must accommodate any lead time.

4.6 SUB-CONTRACT

Approval must be obtained from CIA at the time of quoting for any operations that will be sub-contracted by the PCB supplier. The supplier must provide the name of the sub-contractor(s) and the reason why the operation(s) is being sub-contracted. A quality control system (include qualification of sub-contractor, in-process control plan, incoming inspection etc.) for sub-contract must be applied to ensure sub-contractor offer conforming service. CIA keep the right to audit the sub-contractor in any time.

4.7 PROCESS CHANGES

CIA must be notified in advance for any process changes. This includes:
--Any changes to the fabrication process (includes changes to sequence of operations).
--Any equipment changes.
--Any material changes.
--Any chemistry changes.
All this change can not be appllied until get official approval from CIA.

4.8 REWORKING

4.8.1 The following reworking actions must be approved by CIA

a. Laminate;
b. PTH;
c. Plating;
d. Soldermask.

4.8.2 Requirements for Reworked Parts

a.The procedure for performing any rework must be documented.
b. Reworked parts must be 100% inspected by the supplier.
c. Reworked parts must be traceability.
d. Special packaging must be required.

4.9 REPAIRS

4.9.1 Repair for Conductive Pattern

a. The PCBs with controlled impedance must be no repairs (welds) for conductor, including external layers and inner layers.

b. Inner layers of common multilayer must be no any repairs for conductor.

c. External layers of common multilayer could be repaired for conductor, but must meet following conditions:
--Length of conductor break shall not exceed 0.5 mm.
--Repairs must be coated with soldermask.
--Repairing is not allowed for parallel conductors.
--Open circuit repairs must not encroach onto component mounting pads for lands, test points or connector contact fingers.
--Maximum repairs for each panel must not exceed 1 conductor.
--Maximum repairs for each lot must not exceed 2%.

Notes: The repaired board must be re-Etested after repair. Mechanical repairs or re-welding of the plated holes are not allowed.

4.9.2 Repair for Soldermask

a. Maximum repair for soldermask must not be exceeded 10mm * 10mm.

b. Maximum repairs for each panel must not exceed 2 conductors.

c. Maximum repairs for each lot must not exceed 3%.

4.10FINAL VISUAL INSPECTION

The following requirements must be followed in final inspection.

a. General inspection is to be performed with 100% visual inspection, using a minimum of 3X magnification is suggested.

b. All defects are to be verified at a minimum of 10X magnification.

c. This specification and IPC-A-600 latest version must be referred during visual inspection.

4.11 CERTIFICATE OF CONFORMANCE (COC)

4.11.1 General

For each individual part number, the Certificate of Conformance must be submited with the shipment as a statement.

4.11.2 Required Contents for COC

The following contents must be stated on the Certificate of Conformance:
--The supplier name and product type of CCL used to the shipped goods.
--The supplier name and product type of Solder Mask used to the shipped goods.
--The supplier name and product type of Peelable soldermask used to the shipped goods.
-- UL file number of PCB supplier and CCL supplier must be shown on COC.

4.12 FINAL AUDIT REPORT

4.12.1 General

For each individual part number, the Final Audit Report must be done and submited with the COC and shipment.

4.12.2 Required Contents for Final Audit Report

Following contents must be performed during insection, and which results must be shown on the report:
--Visual Inspection.
--Measurement for Finished Board Thickness, Peelable Solder Mask Thickness, Bow and Twist, Outline Dimension, Minimum Line Width and Hole Diameter.
--Measurement for Controlled Impedacne.
--Cross-section Measurement; (Cu plating Thickness in hole and surface, solder mask thickness, Copper foil thickness)
--Thermal Stress Test.
--Solderability Test.

4.12.3 Cross-setion

a. The Cross-section must be done for each lot and also submitted with the Final Audit Report .

b. The following attributes should be tested along with cross-section.
--Thermal stress
--Continuity of inner layer connections
-- Layer registration
-- Integrity of board lamination
-- Etch back
-- Plating thickness in holes
-- Plating thickness on surface
-- Solderable finish thickness in holes
-- Solderable finish thickness on surface
-- Base copper foil thickness on each layer
-- Dielectric spacing between each layer
-- Dielectric material thickness

4.12.4 Solderability Test Sample

a. The Solderability Test must be done for each lot and the test sample also must be submitted with each Final Audit Report .

4.12.5 Controlled Impedance Test Conpon

See 4.2.2.

4.13 CRITERIAL OF ACCEPTANCE

For each lot before outgoing, CIA require to perform the Shipment Inspection as receiveing inspection. The sampling quantity for Shipment Inspection will be fixed as following

a. Visual Inspection:
MIL-DTD-105, simple sampling plan for ordinary test, Level (II).
AQL : Maj: 0.10; Min: 0.25

b. Dimension Characteristics
Sampling Size: 5 panels for production inspection, 2 panels for sample inspection.
AQL: Acc=0; Rej=1.

c. Performance Characteristics
Sampling Size: 1 panel for production inspection and sample inspection.
AQL: Acc=0; Rej=1.